國 立 臺 北 科 技 大 學

九十七學年度研究所碩士在職專班(含EMBA)入學考試

電腦與通訊研究所
甲組：計算機結構試題

填准考證號碼

第一頁　共一頁

注意事項：

1. 本試題共6題，配分共100分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。

1. (15%) (a) What is called 3C's misses for cache memory design. (5%) (b) How to reduce them ? Explain your design techniques as many as you can. (10%)

2. (20%) A compiler designer is trying to decide between two codes sequences for a particular machine. The hardware designers have supplied the following facts:

Instruction class	CPI for this instruction class
A	1
B	2
C	3

For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code sequence	Instruction count for instructions class		
	A	B	C
1	2	1	2
2	4	1	1

(a) What is the definition of CPI ? (5%) (b) Which code sequence executes the most instructions ? (5%) (c) Which will be faster ? (5%) (d) What is the CPI for each sequence ? (5%)

3. (15%) Assume an instruction cache miss rate for gcc of 5% and a data cache miss rate of 10%. If a machine has a CPI of 4 without any memory stalls and the miss penalty is 12 cycles for all misses, determine how much faster a machine would run with a perfect cache that never missed. Use the frequency of loads and stores is 33% here.

4. (15%) Suppose we have a benchmark that executes in 100 seconds of elapsed time, where 90 seconds is CPU time and the rest is I/O time. If CPU time improves by 50% per year for the next five years but I/O time does not improve, how much faster will occur program run at the end of five years ?

5. (15%) Design a digital circuit which computers the sum of a stream of input numbers and counts the number of input receivers. (a) Develop an algorithm for the processing procedure. (5%) (b) Design a simple data-path with control signals identified. (5%) (c) Define the controller using finite-state machine and give an implementation. (5%)

6. (20%) (a) What is a TLB ? Is it necessary to flush the TLB when processor performs a context switching ? Why ? (10%) (b) How to handle a TLB miss ? (10%)