國立臺北科技大學

九十六學年度電腦與通訊研究所碩士在職專班入學考試

甲組：計算機結構　試題

填准考證號碼

注意事項：

1. 本試題共【7】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。

1. Let a computer have a cache, main memory, and a hard disk used for virtual memory. If a referenced word is in the cache, 25 ns are required to access it. If the word is in main memory but not in the cache, 125 ns are needed to load it to the cache, and then the reference is started again. If it is not in memory, 3.2 ms are required to fetch it from the hard disk, followed by 125 ns to copy it to the cache, and then starts the reference again.

   Suppose that the cache hit ratio is 0.8, and the main-memory hit ratio is 0.55. Calculate the *average time* (in μs) required to access a referenced word on this system. (14%)

2. (a) State how the *demand paging* scheme is used for multiprogramming. (12%)

   (b) Describe the impact of *thrashing* on a multiprogramming system.

3. A process references 5 pages, P, Q, R, S, and T, in the following order: (10%)

   P→R→T→R→Q→S→T→Q→P→R→S→T→S→R→T.

   Given that the replacement policy is first-in-first-out, FIFO, and the above references are started with an empty main memory with 3 page frames. Find the number of the *page faults* and the *page hit ratio*, respectively.

4. The operations of the CPU must be somehow *synchronized* with the low-speed I/O devices. For this synchronization, three techniques have been devised as follows: (18%)

   (a) *Programmed I/O*,

   (b) *Interrupt-driven I/O*,

   (c) *DMA*.

   For each technique, (a)-(c), state how the CPU is synchronize with I//O devices to perform transferring data, respectively.

5. (a) Convert the following formula from infix to *reverse Polish* notation. (12%)

   $$(A+B)\times C-(D+(E-F)\div G)$$

   (b) By stack-based algorithms, calculate the value of the following expressing:

   $$ABC+-DE\div F\times G-+$$

   , represented in *postfix* notation, where $A=D=10$, $B=E=5$, $C=F=2$, and $G=12$.

6. The time delays in the 5 stages of the *instruction pipeline* are as follows: (16%)

   $\tau_1=40$ ns, $\tau_2=38$ ns, $\tau_3=45$ ns, $\tau_4=90$ ns, and $\tau_5=42$ ns.

   The time delay of a latch (or register) advancing data to the next stage is $\tau_r=5$ ns.

   (a) Determine the total time required for the 5-stage pipeline to execute 200 instructions.

   (b) Show a way to reduce the total time, required to perform 200 instructions, to about *one-half* of the time derived in part (a). Justify your answer.

7. (a) What is the *advantage* of the *Booth's* algorithm on multiplication. (18%)

   (b) Use the *Booth's* algorithm to perform the multiplication: $5_{10}\times -7_{10}$, where each number is represented using 5 bits.