國立臺北科技大學

九十四學年度電腦與通訊研究所碩士在職專班入學考試

甲組：計算機結構 試題

填准考證號碼

注意事項：

1. 本試題共【7】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。

1. The time delays of the four segments in the pipeline are as follows: $t_1 = 45$ ns, $t_2 = 35$ ns, $t_3 = 95$ ns, and $t_4 = 50$ ns. The interface register delay time $t_r = 5$ ns.
   (a) How long would it take to add 120 pairs of numbers in the 4-segment pipeline? **(5%)**
   (b) How can you reduce the total time to about one-half of the time derived in part (a)? Verify your answer. **(10%)**

2. (a) Give an example of program that will cause a branch penalty in a 3-segment pipeline, as follows. **(10%)**

   I: Instruction fetch
   A: ALU operation
   E: Execute instruction.

   (b) Give an example to illustrate how to solve the branch penalty in part (a). **(10%)**

3. The access time of cache and main memory, T_c and T_m, are 90 and 1100 ns, respectively. Assume that 75 percent of the memory requests are for *read* and the remaining are for *write*. The hit ratio for read memory only is 0.80. A write-through procedure is used.
   (a) What is the average access time of the system for only memory *read* cycles? **(5%)**
   (b) What is the average access time of the system for both *read* and *write*? **(5%)**
   (c) What is the hit ratio taking the *write* cycles into account? **(5%)**

4. A computer system with a 32-bit address has a 32K-byte cache memory. Each cache block size is 16 bytes. Draw the configurations of caches that are (a) and (b), respectively.
   (a) direct-mapped, (10%)
   (b) four-way set-associated. (10%)
   Please clearly indicate the relationships between the 32-bit addresses and cache addresses.

5. Compare the advantages and disadvantages between RISC and CISC. (10%)

6. Organize a complete 256K-byte memory system with 32K-byte RAM modules. (10%)

7. Describe the purpose of *snoopy cache controller* used in a memory system. (10%)