國立臺北科技大學九十九學年度碩士班招生考試

系所組別：2210 電腦與通訊研究所甲組

第二節　計算機結構　試題

注意事項：

1. 本試題共 5 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Please explain each of the following hardware: SISD, SIMD, MISD, MIMD, and SPMD. List the examples of these architectures. (10 points)

2. What are the differences among polling, interrupt-driven I/O, and DMA? Please explain these methods and under what conditions should these methods be used. (12 points)

3. The following table shows the bit pattern which is an IEEE 754 standard single precision floating point number.

1100 0101 0100 1001 0011 0000 0000 0000

Please write down the related decimal number. (10 points)

4. The performance of an 800MHz processor P is measured by executing 100,000,000 instructions of benchmark code, which is found to take 0.125s. Find the MIPS and CPI for the processor P for this performance experiment. (10 points)

5. A MIPS pipelined processor consists of five pipeline stages: Instruction Fetch (IF), Instruction Decode and Register Read (ID), Execution or Address calculation (EXE), Data Memory Access (MEM), and Register Write Back (WB). Assume that individual stages of the data path have the following latencies:

IF	ID	EXE	MEM	WB
2.5ns	2ns	5ns	2.5ns	1.5 ns

The following MIPS code is executed on a pipelined processor with full forwarding, and a predict-taken branch predictor:

```
Label1:  lw  $1 ,40($6)
         sub $2 , $1 , $4
         beq $2 , $3 , Label2 ; Taken
         add $1 , $1 , $2
Label2 :  beq $1 , $2 , Label1 ; not Taken
         sw  $2 , 20($4)
         and$1 , $2 ,$4
```

(1)What is the clock rate of this 5-stage MIPS pipelined processor? (5 points)

(2)What kind of instruction sequence will cause data hazard that cannot be resolved by full forwarding? Please find out the problems from the given MIPS code and illustrate the related situation and performance penalty. (5 points)

(3)The designers add one pipeline stage in a MIPS processor without any delay penalty and changing the location of existing pipeline registers. What is the maximum clock rate of the 6-stage processor? Please describe which pipeline stage should be designed. (5 points)

(4)Repeat the analysis in (2) for the 6-stage processor. Compare the design of 5-stage and 6-stage processors, when the instruction sequence causes data hazard that cannot be resolved by full forwarding. (5 points)

(5)Give an example of structural hazard in a 5-stage MIPS pipelined processor. (5 points)

(6)Please explain delayed branch technique. (5 points)

(7)Please explain 2-bit branch prediction technique. (6 points)

(8)Draw the 5-stage MIPS pipeline execution diagram for this MIPS code, assuming there are no delay slots and that branches execute in EXE stage. (10 points)

(9)Repeat the analysis in (8) for the 6-stage processor. Draw the 6-stage MIPS pipeline execution diagram for this MIPS code, assuming there are no delay slots and the branch resolving point is advanced from EXE stage to ID stage. (12 points)