國立臺北科技大學九十九學年度碩士班招生考試

系所組別：2401 光電工程系碩士班

第三節　電子學　試題（選考）

注意事項：

1. 本試題共 6 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Consider a full-wave bridge rectifier circuit, as shown in Fig.1, to design a dc power supply that provides an average dc output voltage of 15 V on which a maximum of ±1 V ripple is allowed. The rectifier has a load of resistance R =150 Ω. The rectifier is fed from the line voltage120 V, 60 Hz through a transformer. The diodes available have 0.7-V drop when conducting.
   (a) Find the required value of the filter capacitor C. (5%)
   (b) Find the maximum reverse voltage that will appear across the diode. (5%)
   (c) Calculate the average current through the diode during conduction. (5%)

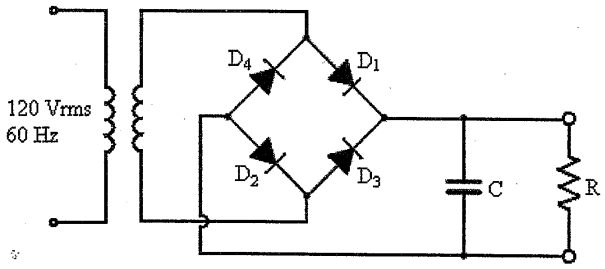

Fig. 1

2. For the circuit in Fig. 2, find the base voltage V_B and the emitter voltage V_E of the transistors Q_1 and Q_2 when the input voltage v_I equals to (a) +3 V (b) –5 V and (c) –10 V. The BJTs have current gain β =100 when they are biased in active mode. (15%；each 5%)

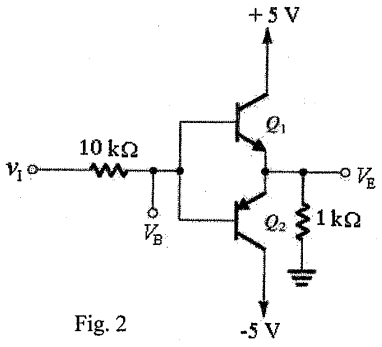

Fig. 2

3. In Fig. 3, consider a three-stage amplifier in which the stages are directly coupled. Assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.
   (a) Consider the dc bias current in each of the three transistors and then find the dc voltage at the output. Assume the base to emitter voltage | V_{BE} | =0.7 V and current gain β =100 for the BJTs biased in active mode, and neglect the Early effect. (5%)
   (b) Find the input resistance and the output resistance. (5%)
   (c) Use the current-gain method to find the voltage gain v_o / v_i. (5%)
   (d) Find the frequency of the high-frequency pole formed at the interface between the first and the second stages. Assume that $C_{\mu 2}$ =2 pF and $C_{\pi 2}$ =10 pF. (5%)

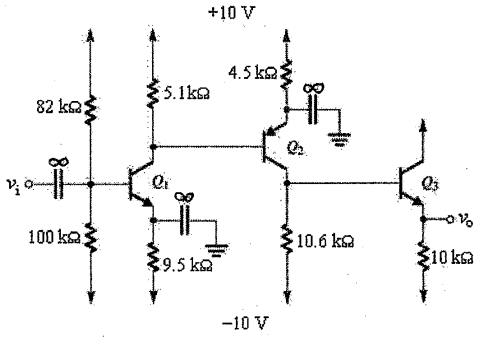

Fig. 3

注意：背面尚有試題

4. For the shunt-series feedback amplifier of Fig. 4, derive expressions for current gain A_f $=I_o/I_s$ and input resistance R_{in}. Neglect r_o and the body effect. (15%)

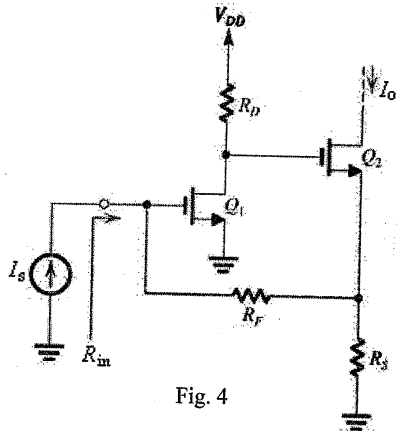

Fig. 4

5. The differential amplifier circuit of Fig. 5 utilizes a resistor connected to the negative power supply to establish the bias current I.

(a) For $v_{B1}= v_{id}/2$ and $v_{B2}= -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $| v_o/ v_{id} |$. (5%)

(b) For $v_{B1}= v_{B2}= v_{icm}$, find the magnitude of the common-mode gain, $| v_o/ v_{icm} |$. (5%)

(c) Calculate the CMRR. (5%)

(d) If $v_{B1}= 0.1 \sin 2\pi\times 60t + 0.005 \sin 2\pi\times 1000t$ volt and $v_{B2}= 0.1 \sin 2\pi\times 60t - 0.005 \sin 2\pi\times 1000t$ volt, find v_o. (5%)

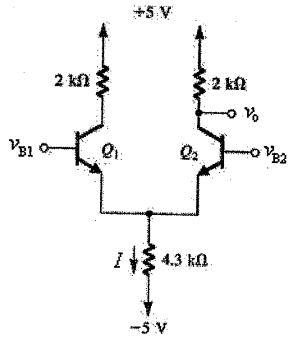

Fig. 5

6. Consider the circuit in Fig. 6. (a)Break the feedback loop at node X and find the loop gain $A\beta = V_o(j\omega)/ V_x(j\omega)$. (b)Find the minimum value R_f for oscillation to start. (c) Find the frequency of oscillation f_o. (15%；each 5%)

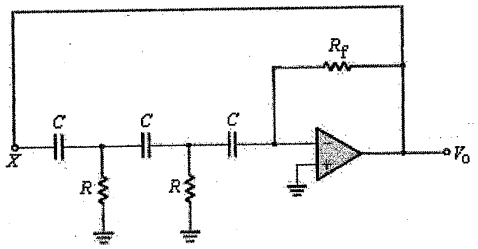

Fig. 6