# 國立臺北科技大學九十八學年度碩士班招生考試

## 系所組別：2240 電腦與通訊研究所丁組

## 第一節　數位邏輯設計　試題



**注意事項：**

1. 本試題共五題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一. Simplify the following Boolean expressions, using theorem and rules of Boolean algebra. Draw the logic circuits of the un-simplified and simplified expressions.

1. $Y=(\overline{A+B})CD+(\overline{A+B})$ (10%)

2. $W=(PQR+\overline{PQ})(S+T)+(\overline{P}+\overline{Q})(S+T)+(S+T)$ (10%)

二. Draw a circuit that uses an 8-to-1 multiplexer to generate a programmable 8-bit repeating pattern. Draw the timing diagram of the select inputs and the output waveform for the following pattern of data inputs.
$D_7$=1, $D_6$=0, $D_5$=1, $D_4$=0, $D_3$=0, $D_2$=1, $D_1$=1, $D_0$=0 (20%)

三. Which of the following sums will produce a sign bit overflow in 8-bit 2's complement notation? How can you tell? (20%)

1. $67_{10}+33_{10}$
2. $67_{10}+63_{10}$
3. $-96_{10}-22_{10}$
4. $-96_{10}-42_{10}$

四. Derive the synchronous input equations of a 4-bit synchronous binary counter based on D flip-flops. Draw the corresponding counter circuit. (20%)

五. A state machine called a single-pulse generator operates as follows:
The circuit has two states: **seek** and **find**, an input called **sync** and an output called **pulse**. The state machine resets to the state **seek**. If **sync**=1, the machine remains in **seek** and the output, **pulse**, remains LOW. When **sync**=0, the machine makes a transition to **find**. In this transition, **pulse** goes HIGH. When the machine is in state **find** and **sync**=0, the machine remains in **find** and **pulse** goes LOW. When the machine is in **find** and **sync**=1, the machine goes back to **seek** and **pulse** remains LOW. Use classical state machine design techniques to design the circuit for the single-pulse generator, using D flip-clops for the state logic. Briefly describe what this state machine does. (20%)