國立臺北科技大學九十八學年度碩士班招生考試

系所組別：2210 電腦與通訊研究所甲組

第二節 計算機結構 試題

注意事項：

1. 本試題共八題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、Let the processors *P*1 and *P*2 be designed with CISC and RISC, respectively. Using a typical benchmark program, the machine characteristics of processors are listed as follows.

Processor	Clock Rate	Performance	CPU time
*P*1 (CISC)	30 MHz	1.6 MIPS	12.5 x seconds
*P*2 (RISC)	125 MHz	20 MIPS	1.35 x seconds

(a) Compute the ratio of the instruction counts of *P*2 to *P*1, executing machine codes for the benchmark program. (5%)

(b) Calculate the ratio of the average CPI values of *P*1 to *P*2. (5%)

二、Suppose that a 10-bit data word stored in memory is **1101001011**.

(a) Using the Hamming algorithm, determine what *check bits* would be stored in memory with the data word. Show the layout of 10 data bits and 4 check bits for the data word. (6%)

(b) Given that when the word is read from memory, the 4 check bits are recalculated to be **0101**. What is the 10-bit data word that was read from memory? (6%)

三、What is the difference between *memory-mapped* I/O and *isolated* I/O? (12%)

四、Consider a computer system with both *segmentation* and *paging*. When a segment is in memory, some words are wasted on the last page. Moreover, for a segment size S and a page size P, the system needs S/P page table entries. However, the smaller the page size, the less waste in the last page of the segment, but the larger the page table. What *page size* can minimize the total overhead? (10%)

五、Let an instruction set use a fixed 20-bit instruction length. An operand field occupies 7 bits in length. There are 62 *two*-operand instructions and 256 *zero*-operand instructions. Determine the *maximum* number of *one*-operand instructions that can be supported. (10%)

六、Give an example to illustrate how a *delayed branch* can improve the performance of a RISC pipeline machine. (10%)

七、Consider a uniprocessor with separate *data* and *instruction* caches, with hit ratios of H_d and H_i, respectively. Access time from processor to cache is x clock cycles, and transfer time for a block between memory and cache is y clock cycles. Let F_i denote the fraction of memory accesses that are for instructions.

(a) Determine the effective access time, T_i, only for instruction cache (i.e., $F_i = 1.0$) in terms of the parameters defined as above. (6%)

(b) Given that F_d denotes the fraction of *dirty lines* in the data cache among lines replaced, and apply a *write-back* policy for data consistency. Determine the effective access time, T_e, in terms of the parameters, $0 < F_d, F_i < 1.0$. (10%)

八、(a) Depict the block diagram of hardware implemented for n-bit unsigned binary multiplication, in which the multiplier and multiplicand will be loaded into registers Q ($Q_{n-1} \sim Q_0$) and M ($M_{n-1} \sim M_0$), respectively. (10%)

(b) Assume that the contents of 5-bit registers Q and M are **10111** and **11001**, respectively. Show the process for the 5-bit unsigned binary multiplication, based on the hardware you depicted in part (a). (10%)