# 國立臺北科技大學九十八學年度碩士班招生考試

## 系所組別：2401 光電工程系碩士班不分組

## 第三節　電子學（選考）試題



**注意事項：**

1. 本試題共六題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一. 10%

In a forward-biased *pn* junction show that the ratio of the current component due to hole injection across the junction to the component due to electron injection is given by

$$\frac{I_p}{I_n}=\frac{D_p}{D_n}\frac{L_n}{L_p}\frac{N_A}{N_D}$$

Evaluation this ration for the case $N_A = 10^{18}/\text{cm}^3$, $N_D = 10^{16}/\text{cm}^3$, $L_p = 5$ μm, $L_n = 10$ μm, $D_p = 10$ cm$^2$/s, $D_n = 20$ cm$^2$/s, and hence find $I_p$ and $I_n$ for the case in which the diode is conducting a forward current $I = 1$ mA.

二. 20%

A short-base diode is one where the widths of the p and n regions are much smaller than $L_n$ and $L_p$, respectively. As a result, the excess minority-carrier distribution in each region is a straight line rather than the exponentials shown in Fig. 1.

1. For the short-base diode, sketch a figure corresponding to Fig. 1, and assume, as in Fig. 1, that $N_A >> N_D$. (5%)
2. Show that if the widths of the *p* and *n* regions are denoted $W_p$ and $W_n$ then

$$I = Aqn_i^2\left[\frac{D_p}{(W_n-x_n)N_D}+\frac{D_n}{(W_p-x_p)N_A}\right]\left(e^{V/V_T}-1\right)$$

and

$$Q_p=\frac{1}{2}\frac{(W_n-x_n)^2}{D_p}I_p\cong\frac{1}{2}\frac{W_n^2}{D_p}I_p, \text{ for } W_n >> x_n. \text{ (5%)}$$

3. Also, assuming $Q \cong Q_p$, $I \cong I_p$, show that

$$C_d=\frac{\tau_T}{V_T}I$$

where

$$\tau_T=\frac{1}{2}\frac{W_n^2}{D_p}. \text{ (5%)}$$

4. If a designer wishes to limit $C_d$ to 8 pF at $I = 1$ mA, what should $W_n$ be? Assume $D_p = 10$ cm$^2$/s. (5%)

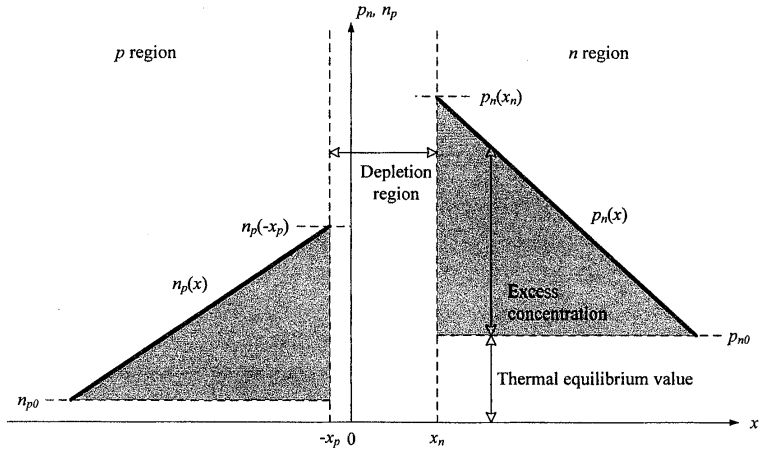


***Figure 1***

三. 20%

Figure 2 shows a MOS amplifier. The MOSFET is biased at $I_D = 1.06$ mA and has $g_m = 0.725$ mA/V and $r_o = 47$ kΩ. The midband analysis showed that $V_o/V_i = -3.3$ V/V and $R_{in} = 2.33$ MΩ. Select appropriate values for the two capacitors so that the low-frequency response is dominated by a pole at 10 Hz with the other pole at least a decade lower.

注意：背面尚有試題

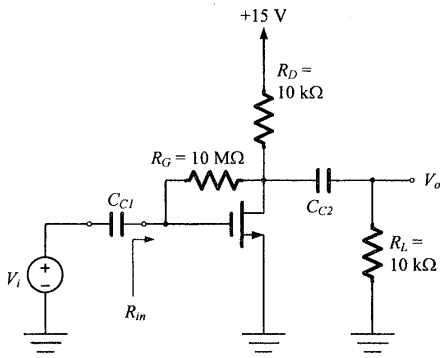


***Figure 2***

四. 20%

1. Sketch a CMOS realization for the function $Y = \overline{A + B(C + D)}$. (10%)
2. Sketch a pseudo-NMOS realization of the exclusive-OR function $Y = A\overline{B} + \overline{A}B$. (10%)

五. 20%

For the circuit of the figure 3, the op amplifier has open-loop gain $A_d$ = $10^4$ V/V, differential input resistance $R_{id}$ = 100 kΩ, and incremental output resistance $r_o$ = 1kΩ. Please use the feedback method to find

1. the voltage gain $V_o/V_s$. (5%)
2. the input resistance $R_i$, (5%) and
3. the output resistance $R_o$. (5%)
4. What is the configuration of the feedback amplifier? (5%)

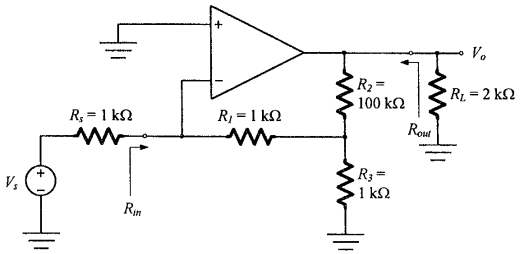


***Figure 3***

六. 10%

The active biquard filter as shown contains passive elements and ideal operational amplifiers, as shown in figure 4. Please derive the transfer functions of $V_o$(s)/$V_i$(s).

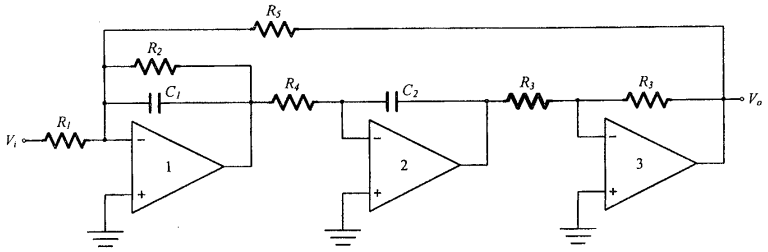


***Figure 4***