國立臺北科技大學九十七學年度碩士班招生考試

系所組別：2240 電腦與通訊研究所丁組

第二節　電子學　試題

填 准 考 證 號 碼

注意事項：

1. 本試題共七題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Assume each diode in the circuit shown in Fig.1 has a cut-in voltage of $V_\gamma = 0.65$V.
   (a) The input voltage is $V_I = 5$V. Please calculate the value of R_1 required such that I_{D1} is one-half the value of I_{D2}. (5%)
   (b) If $V_I = 8$V and $R_1 = 2$ kΩ, please calculate the current I_{D1} and I_{D2}. (10%)

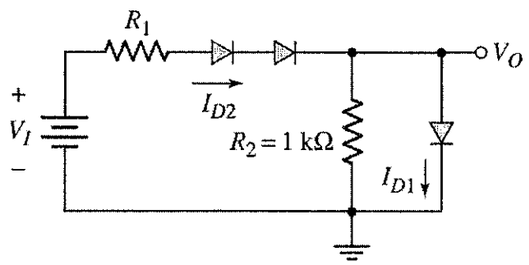


Fig.1 Diode circuit for problem 1

2. Now we want to design the common-base circuit shown in Fig. 2 such that $I_{EQ} = 0.50$mA and $V_{ECQ} = 4.0$V. Assume transistor parameters of $\beta = 120$ and $V_{EB}(\text{on}) = 0.7$V.
   (a) Determine the value of R_E. (5%)
   (b) Calculate the value of I_{CQ}. (5%)
   (c) Determine the value of R_C. (5%)

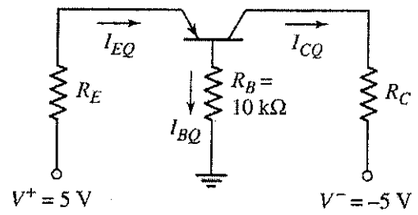


Fig.2 Circuit for problem 2

3. Now assume $V_\gamma = 0.7$V for each diode in the circuit in Fig. 3. Please plot v_o versus v_I for $-10\text{V} \leqq v_I \leqq +10\text{V}$. Indicate the breakpoints and give the state of each diode in the various regions of the plot. (You should make clearly the voltage levels and timing information on your plot.) (15%)

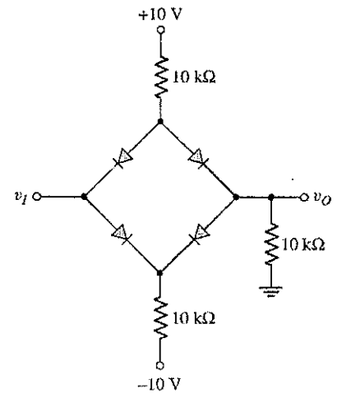
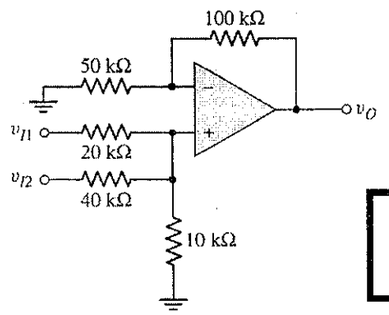


Fig.3 Diode circuit for problem 3

4. Consider the ideal noninverting op-amp circuit in Fig. 4.
   (a) Derive the expression for v_O as a function of v_{I1} and v_{I2}. (10%)
   (b) Find the value of v_O for $v_{I1} = +0.25$V and $v_{I2} = -0.40$V. (5%)



注意：背面尚有試題

Fig.4 Noninverting op-amp circuit for problem 4

5. For the circuit in Fig. 5, assume transistor parameters of $\beta = 100$ and $V_{BE}(\text{on}) = 0.7\text{V}$.
   （a）Find Thevenin voltage (V_{TH}) and Thevenin resistance (R_{TH}) for the base circuit. （10%）
   （b）Determine the value of I_{CQ} and V_{CEQ}. （10%）

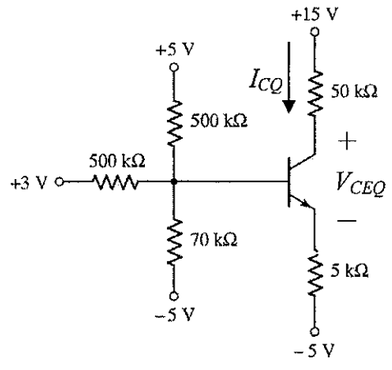


Fig. 5 Circuit for problem 5

6. A CMOS inverter with square wave input and RC load is shown in Fig. 6.
   (a) Please analyze the power consumption of the CMOS inverter. （5%）
   (b) A CMOS inverter is biased at $V_{DD} = 3\text{V}$. The inverter drives an effective load capacitance of $C_L = 0.5$ pF. Determine the maximum switching frequency such that the power dissipation is limited to $P = 0.10\ \mu$ W. （5%）

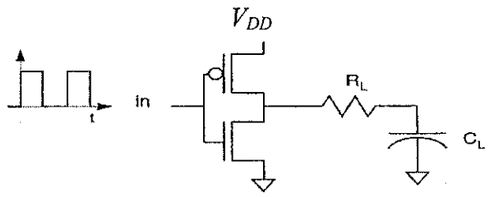


Fig. 6 CMOS inverter circuit for problem 6

7. Fig. 7 shows a dynamic logic NAND3 circuit example with function $f = \overline{a \bullet b \bullet c}$. Please use this circuit to explain the "charge sharing" problem. （10%）

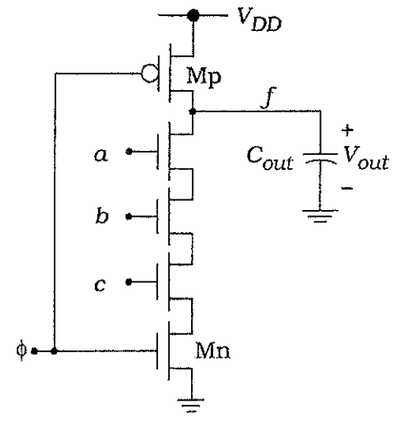


Fig.7 Dynamic logic NAND3 circuit for problem 7