國立臺北科技大學九十七學年度碩士班招生考試

系所組別：2210 電腦與通訊研究所甲組

第二節　**計算機結構**　試題

填 准 考 證 號 碼

注意事項：

1. 本試題共七題，配分共 **100** 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、Let a benchmark program be run on a 150 MHz processor. The object code consists of 10,000 instructions, with the following instruction mix and clock cycle count. (9%)

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	4,800	1
Data transfer	3,250	2
Control transfer	750	2
Floating point	1,200	4

Determine the effective CPI, MIPS rate, and execution time in ms for this program.

二、A computer is equipped with a byte addressable main memory of 2^{20} bytes and block size of 32 bytes. Assume that a direct mapped cache consisting of 256 lines is used with this computer.

(a) How is a 20-bit memory address divided into *tag*, *line number*, and *byte number*? (4%)

(b) Into what line would bytes with each of the following addresses be stored?

(i) **2D2B2**h (2%)

(ii) **A068E**h (2%)

(c) Suppose the byte with address **6BAD5**h is stored in the cache. What are the addresses of the other bytes stored along with it? (4%)

(d) How many total bytes of main memory can be stored in the cache? (4%)

三、Consider a single-platter disk with the following parameters: Rotation speed: 7,500 rpm (revolutions per minute); Number of tracks on one side of platter: 25,000; Number of sectors per track: 500; Seek time: 1.3 ms for every 100 tracks traversed.

Assume that the disk driver receives an I/O request to access a random sector on a random track and the disk head starts at track zero.

(a) What is the average seek time? (3%)

(b) What is the average rotation latency? (3%)

(c) What is the transfer time for a sector? (3%)

(d) What is the total average time to satisfy an I/O request? (3%)

四、List and briefly describe three techniques used for performing I/O data transfer. (15%)

五、Suppose the page table for some process currently executing on the processor is as follows. All addresses are memory byte addresses, and everything is numbered starting from zero. The page size is 2^{11} bytes.

Virtual page No.	Valid bit	Reference bit	Modified bit	Page Frame No.
0	0	0	0	-
1	1	1	1	6
2	0	0	0	-
3	1	0	0	3
4	0	0	0	-
5	1	1	0	0
6	0	0	0	-
7	1	1	1	2

(a) Describe how, in general, a virtual address generated by the CPU is translated into a physical address for accessing main memory. (4%)

(b) What physical address, if any, would each of the following virtual addresses correspond to? (Do not handle any page faults, if any.)

(i) **0E8A**h (4%)

(ii) **16DF**h (4%)

(iii) **3B4C**h (4%)

注意：背面尚有試題

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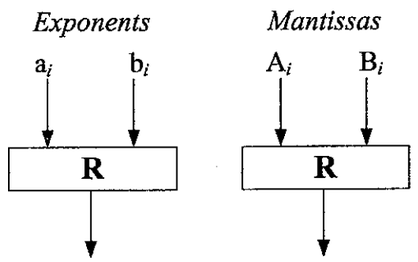
六、Designing pipelines within the ALU can speed up floating-point operations. For floating-point addition and subtraction, the pipeline can be assigned to have two parallel threads, one handling exponents and one handling mantissas, and could start out like this: (16%)



The boxes labeled **R** represent a set of registers holding temporary results. Please complete the whole block diagram to show the structure of the pipeline for floating-point additions and subtractions.

七、The following code segment needs to be executed 128 times for evaluating the vector arithmetic expression: $D(I) = A(I) \times C(I) + B(I) \times C(I)$, $0 \leqq I \leqq 127$.

```
Load R1, A(I)
Load R2, C(I)
Multiply R1, R2
Load R3, B(I)
Multiply R3, R2
Add R1, R3
Store D(I), R1
```

where R1, R2, and R3 denote process registers. Assume 6 clock cycles for each **Load** or **Store**, 3 cycles for the **Add**, and 9 cycles for the **Multiply** on either an SISD computer or an SIMD computer. Processors in both computers are driven by the same-speed clock, 512 MHz.

(a) Compute the total number of clock cycles needed to execute this code segment repeatedly 128 times on an SISD uniprocessor computer sequentially, ignoring all time delays. (5%)

(b) Let an SIMD computer contain 128 processing elements to execute the above vector operations concurrently over 128-component vector data. Calculate the total execution cycles on the SIMD machine, ignoring instruction broadcast and other delays. (5%)

(c) Try to revise the above code segment to shorten the total execution time for the same vector operations. (6%)