國立臺北科技大學九十五學年度碩士班招生考試

系所組別：1111 機電整合研究所甲組

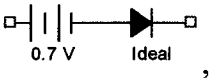
第二節 電子學（選考）試題

填 准 考 證 號 碼

注意事項：

1. 本試題共 4 大題，第 1 大題為填充題共 60 分，第 2、3、4 大題分別為 10、15、15 分，共 100 分。
2. 請按順序標明題號作答，不必抄題，數值答案請提供四位有效數字。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. To each of the blanks below, please sequentially put your answers on your answer sheet. (@6%*10=60%)

(1) If each of the diodes in Fig. 1 can be equivalently expressed as 

, then the current through diode D_2 should be __1.1__ mA.

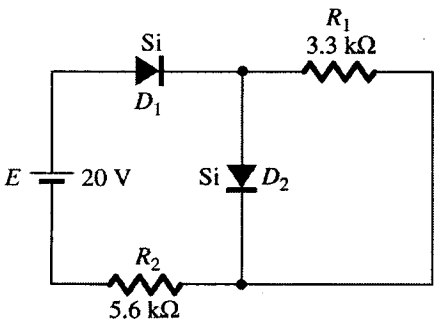


Fig. 1

(2) To the transistor in Fig. 2, the accurate voltage of operating point (or say Q-point), V_{CEQ}, should be __1.2__ V. The accurate input impedance, Z_i, of the circuit should be __1.3__ kΩ.

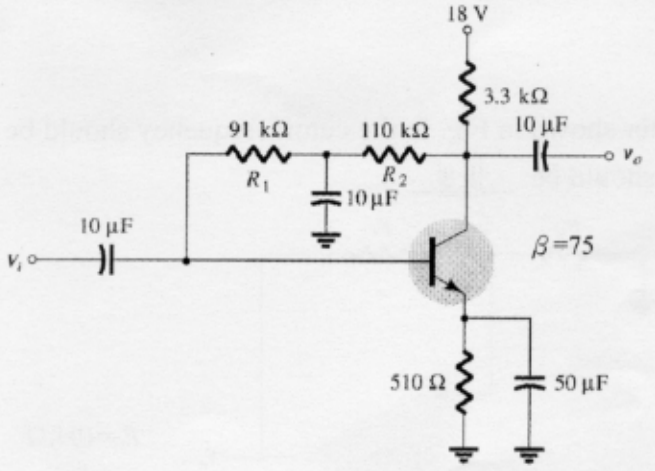
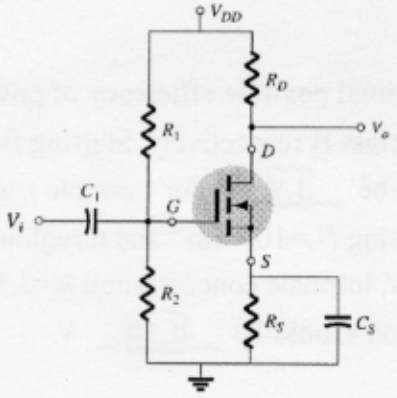


Fig. 2

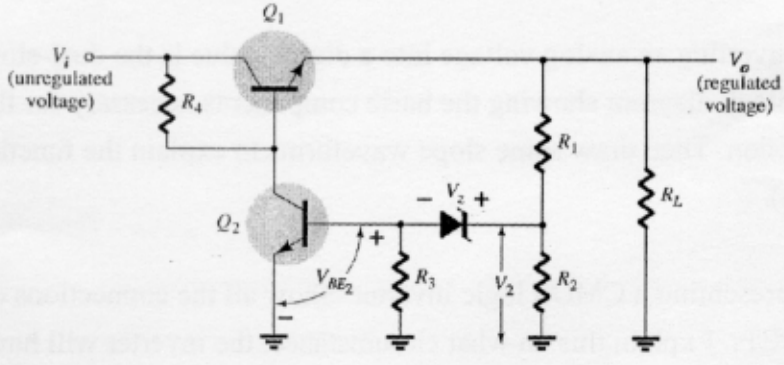
(3) To the transistor in Fig. 3, the accurate drain current of operating point (or say Q-point), I_{DQ}, should be __1.4__ mA. The accurate voltage gain, A_v, of the circuit should be __1.5__ .



V_{DD}=40 V
R_1=22 MΩ
R_2=18 MΩ
R_D=3 kΩ
R_S=0.82 kΩ
$V_{GS(Th)}$=5 V
$I_{D(ON)}$=3 mA at $V_{GS(ON)}$=10 V
y_{os}=20 μ S(output admittance)

Fig. 3

(4) For the circuit in Fig. 4, the regulated voltage, V_o, should be __1.6__ V.

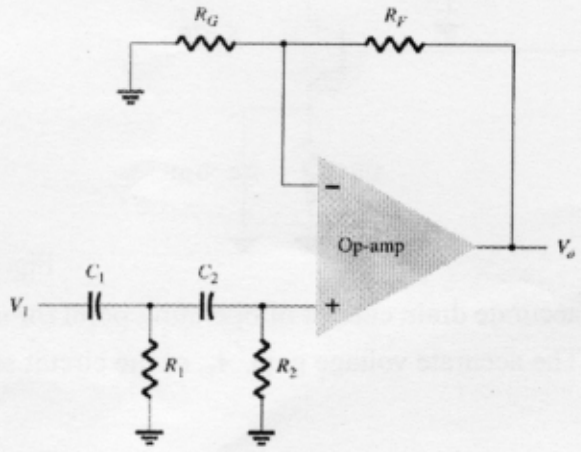


R_1=20 kΩ
R_2=30 kΩ
R_3=30 kΩ
R_4=10 kΩ
V_z=8.3 V

Fig. 4

注意：背面尚有試題

(5) For the active filter shown in Fig. 5, the cutoff frequency should be [1.7] kHz and the voltage gain should be [1.8] .



(b)

R_G=10 kΩ
R_F=50 kΩ
R_1=R_2=2.1 kΩ
C_1= C_2=0.05 μF

Fig. 5

(6) Let η_A, η_{A+T} and η_B represent the maximal possible efficiency of power amplifiers of class A, transformer-coupled class A and class B respectively. Starting from the highest value to the lowest, their sequence should be [1.9] (For example $\eta_A > \eta_{A+T} > \eta_B$).

(7) A p-n junction is formed with p region having N_a=10^{16} cm^{-3} and n region having N_d=10^{17} cm^{-3}. At 27℃ (thermal voltage V_t=0.026 V, intrinsic concentration n_i=1.5*10^{16} cm^{-3}), the build-in potential of the junction's depletion should be [1.10] V.

2. If a diode's current can be expressed as $I_D = I_S(e^{11600V_D/T} - 1)$, please prove that the dynamic resistance r_d can be expressed as $r_d \cong \frac{26mV}{I_D}$ providing that $I_D >> I_S$, $V_D > 0.7$ V and T=300 °K (10%).

3. A popular method of converting an analog voltage into a digital value is the dual-slope method. Please draw a block diagram showing the basic components necessary for the analog-to-digital conversion. Then draw some slope waveforms to explain the functions of the block diagram (15%).

4. Please draw a circuit representing a CMOS logic inverter. Show all the connections of each terminal on MOSFETs. Explain this: at what circumstance, the inverter will have a short circuit current and what factors involve in this unwanted situation (15%).