國立臺北科技大學九十五學年度碩士班招生考試

系所組別：1740 電腦與通訊研究所丁組

第二節 電子學 試題

填 准 考 證 號 碼

注意事項：

1. 本試題共 10 題，配分共 100 分。每題 10 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. The CMOS layout is shown in Fig.1, sketch the corresponding CMOS circuit and what function is provided for this circuit ?

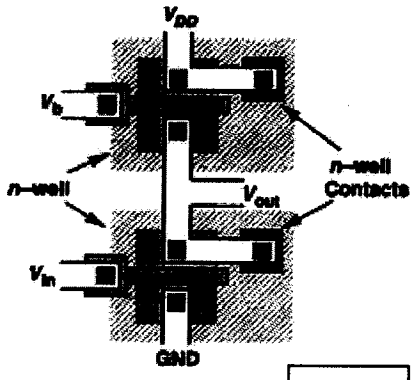

Fig.1

2. In the Fig.2, assume that the transconductance and output resistance of nMOS are g_{mN} and r_{oN}. The transconductance and output resistance of pMOS are g_{mP} and r_{oP}. Find the small -signal differential gain V_{out}/V_{in}.

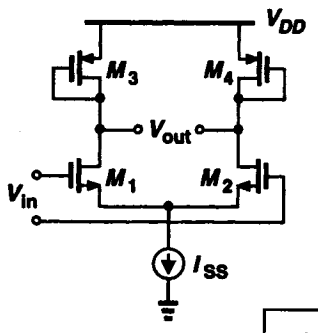

Fig.2

3. In the Fig.3, assume that the transconductances of all MOS are g_m and output resistances of all MOS are infinite. C_{GS1}, C_{GS2}, C_{GD1}, C_{GD2}, C_{DB1}, C_{DB2} and C_{SB2} are the equivalent capacitances of MOS high frequency model. C_L is load capacitance. Use Miller effect to find the three poles of node A, node X and node Y.

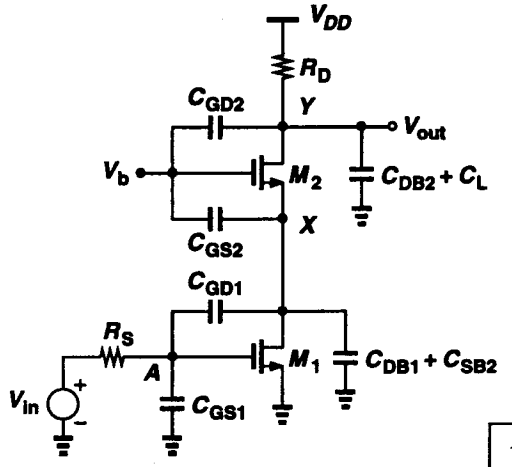

Fig.3

4. In the Fig.4, what type of feedback is used for this circuit ? Assume that the transconductances of MOS are g_m and output resistance is infinite, find the voltage gain V_{out}/V_{in}

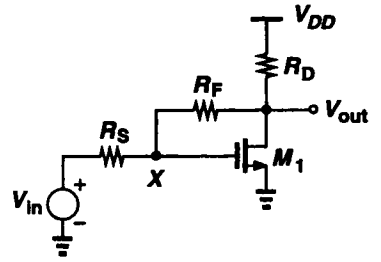

Fig.4

5. In the Fig.5, the closed-loop voltage gain is equal to 10, find the minimum value of A_1 for a gain error of 1%.

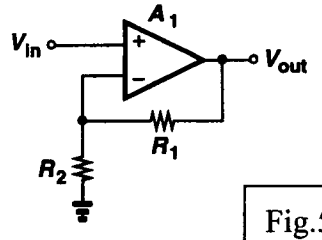

Fig.5

注意：背面尚有試題

6. In the Fig.6, the input signal is V_i , sketch the corresponding block-diagram realization and what functions are provided for the three output voltages in this circuit ?

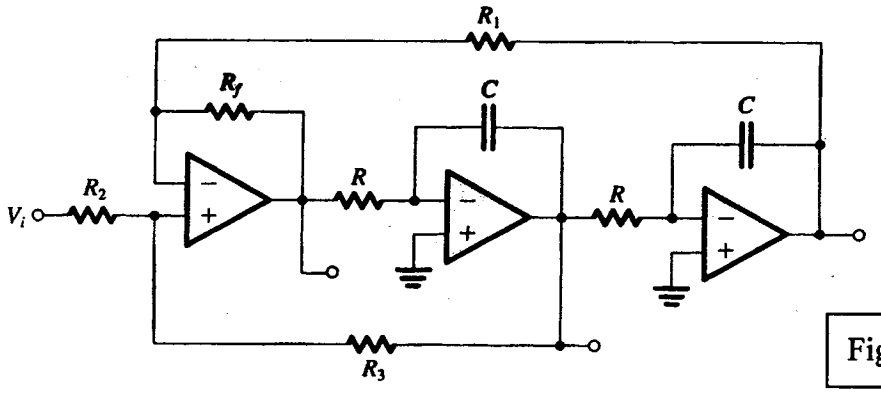

Fig.6

7. In the Fig.7, v_A is assumed to be negative, what function is provided for this circuit and explain the operation principle.

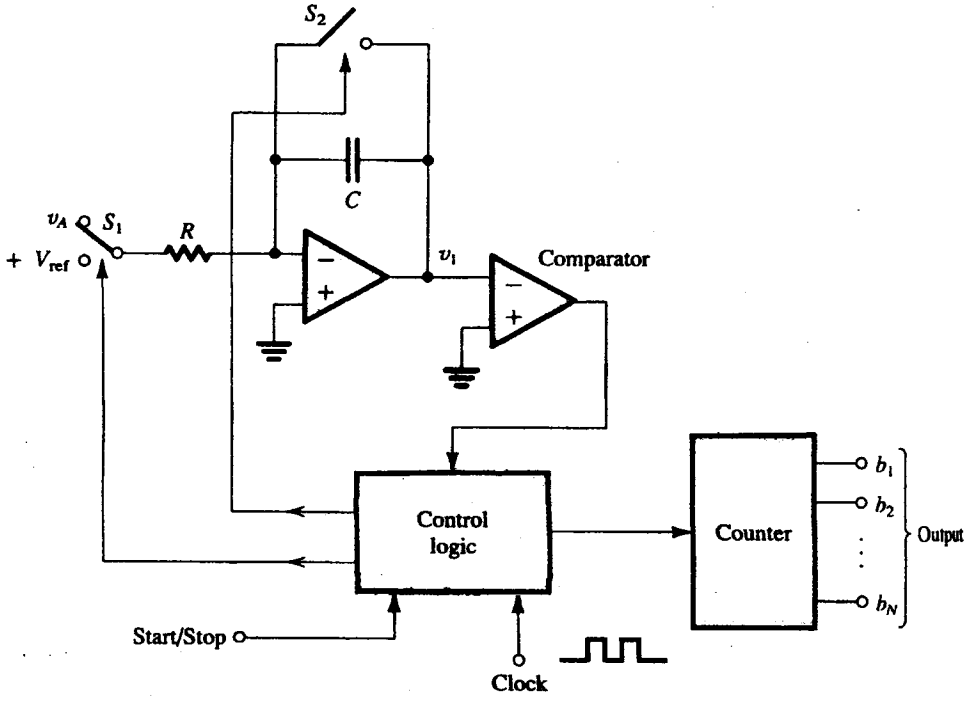

Fig.7

8. In the Fig.8, what function is provided for the V_o in the circuit ? Explain it clearly.

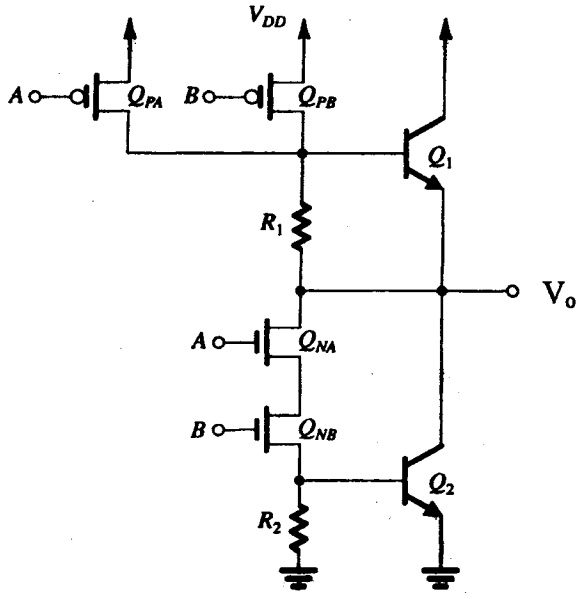

Fig.8

9. In the Fig.9, ϕ is clock, what function is provided for the V_o in the circuit ? Explain it clearly.

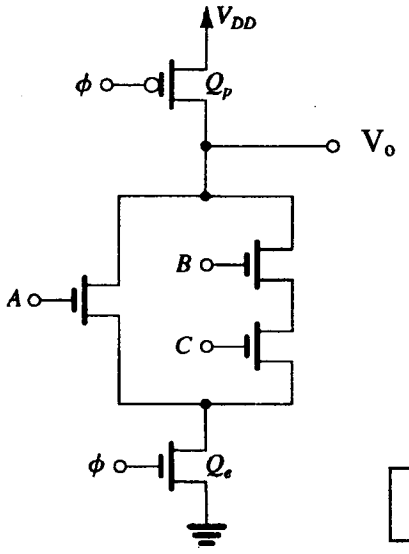

Fig.9

10. Given inputs A, B, C, D, E, design a CMOS logic circuit to implement the logic function Y= (A+B)(C+D)E .