國立臺北科技大學九十五學年度碩士班招生考試

系所組別：1710 電腦與通訊研究所甲組

第二節 計算機結構 試題

填准考證號碼

注意事項：

1. 本試題共六題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。
4. 可攜帶一般型計算機。

1. You are designing the NTUT-I computer and testing it on your audio-video program. The clock rate of this machine is 400MHz. Here are the measures for your audio-video program.

Instructions	CPI	Frequency
X	1	50%
Y	2	25%
Z	4	25%

(a) What is the average CPI for NTUT-I machine when running this program ? (5%)

(b) What is the MIPS rating for the NTUT-I machine when running this program ? (5%)

Suppose we introduce a new address mode and develop a new compiler called the TIT compiler. The address mode will length the clock cycle time by 10% and it along with the TIT compiler can result in the instruction count reductions shown below.

Instructions	% of instruction executed vs. original machine Frequency
X	60%
Y	40%
Z	80%

(c) What is the new average CPI by using new configuration, which are new addressing mode and compiler optimization? (5%)

(d) What is the speedup by using the new configuration ? (5%)

2. Answer following question.

(a) What is a TLB ? Is it necessary to flush the TLB when processor performance a context switching ? Why ? (10%)

(b) How to handle a TLB miss ? (5%)

3. Answer following questions.

(a) Draw and label a hypercube of degree four. (5%)

(b) What is the definition of diameter in the parallel computer ? (5%)

(c) What is the diameter of a hypercube of degree n ? Explain your answer. (5%)

4. Show that IEEE 754 binary representation of the number -0.75_{ten} in single and double precision, respectively. (10%)

5. A computer has a three-level cache used for virtual memory. If a word is in the 1st-level cache, w-ns are required to access it. If it is in the 2nd-level cache but not in the 1st-level, x-ns are first needed to load it into the 1st-level cache, and then the reference is started again. If the word is in the 3rd-level cache but not in the 2nd-level cache, y-ns are required to fetch it from the 3rd-level cache, followed by x-ns to get it to the 1st-level cache. The miss penalty of the 3rd-level cache is z-ns. If the hit ratios for the 1st, 2nd-, and 3rd-level cache are $(p-1)/p$, $(q-1)/q$, and $(r-1)/r$, what is the formula for the average access time for this three-level cache (in terms of w, x, y, p, q, and r) ? (15%)

6. (a)What is the function of the RAID (Redundant Array of Inexpensive Disks) ? (5%)

(b) What is the RAID 3 ? Explain it in details. (10%)

(c) What is the RAID 5 ? Explain it in details. (10%)