國立臺北科技大學

九十四學年度電腦與通訊研究所入學考試

電子學試題

填准考證號碼

注意事項：

1. 本試題共 6 題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. For the diode circuits

(a) Each diode in Fig.1 has piecewise linear parameters of $V_r = 0$ and $r_f = 0$. Plot v_O versus v_I for $0 \le v_I \le +30$ V. Indicate the breakpoints and give the state of each diode in the various regions of the plot. (You should make clearly the voltage levels and timing information on your plot) (10%)

(b) Each diode in Fig.2 has piecewise linear parameters of $V_r = 0.7$V and $r_f = 10\Omega$. Plot v_O versus v_I for $-30 \le v_I \le +30$ V. Indicate the breakpoints and give the state of each diode in the various regions of the plot. (10%)

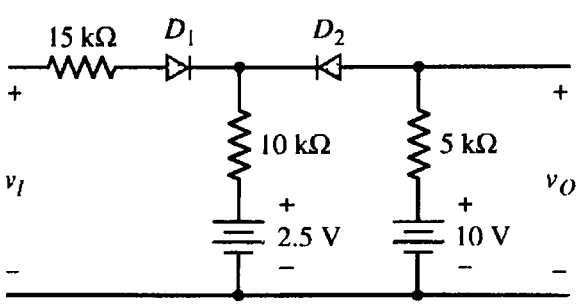

Fig.1 Circuit for problem 1.(a)

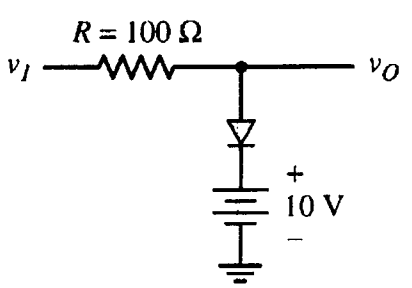

Fig.2 Circuit for problem 1.(b)

2.

（a） Given input A, B, C, D, and E, please design a CMOS logic circuit to implement the logic function Z = A+BC(D+E) with minimum number of transistors. （10%）

（b） Draw a voltage supply circuit with input AC 110 V_{rms} and output of +5V. Please use a full-wave bridge rectifier, capacitor filter, and a three-terminal voltage regulator IC(7805) to provide an output of +5V. （10%）

3.

（a） Consider the Wien-bridge oscillator in Fig.3, please derive the expression for the frequency of oscillation (f_0) and shows the condition for sustained oscillations.（10%）

（b） Fig.4 shows a class AB output stage equipped with protection against the effect of short-circuiting the output. Please describe how the short-circuit protection works and discuss the advantage & disadvantage of this circuit. （10%）

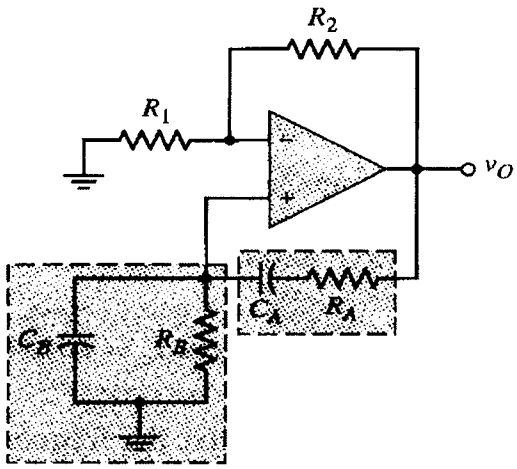

Fig.3 A Wien-bridge oscillator Circuit

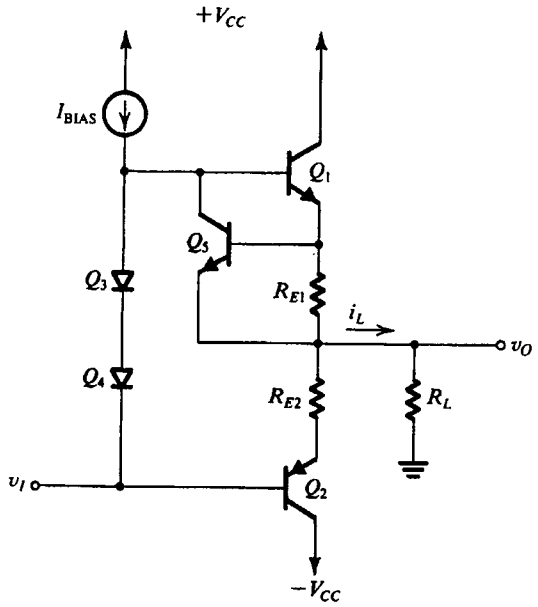

Fig.4 A class AB output stage equipped with short-circuit protection

注意：背面尚有試題

4. Fig.5 shows a voltage-to-current converter. Let Z_L = 100Ω, R_1 = 10kΩ, R_2 = 1Ωk, R_3 = 1kΩ, and R_F = 10kΩ. If v_I = −5V, determine the load current i_L, current i_3 and the output voltage v_O. （15%）

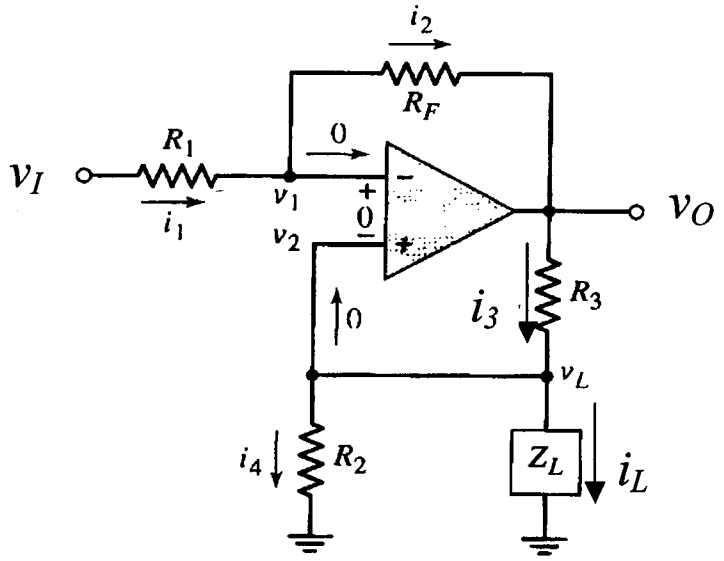

Fig.5 A voltage-to-current converter

5. Fig.6 shows a cross-sectional diagram of a CMOS inverter, please use Fig.6 to explain the latch-up effect in CMOS circuits. (You should make clearly the parasitic elements and effect information on your graph)（10%）

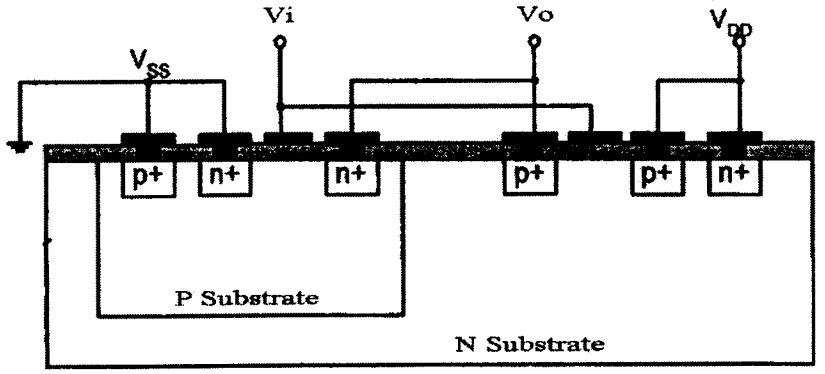

Fig.6 A cross-sectional diagram of a CMOS inverter

6. For the circuit in Fig. 7, assume the transistor parameters are β=100, V_{BE}(on)=0.7V, please calculate the values of V_B、V_C及 I_C. （15%）

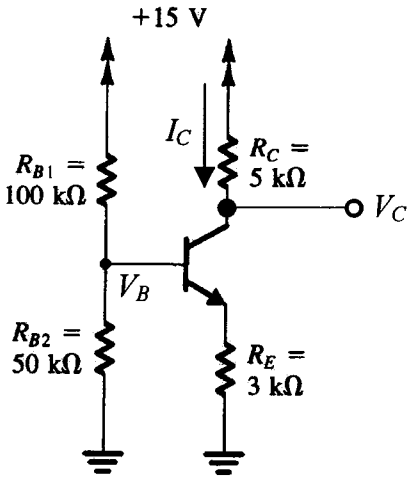

Fig.7 Circuit for problem 6