國立臺北科技大學

九十四學年度電腦與通訊研究所入學考試

計算機結構試題

填准考證號碼

注意事項：

1. 本試題共 5 題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. [20%]

(a) The performance of a 100MHz microprocessor *P* is measured by executing 10,000,000 instructions of benchmark code, which is found to take 0.25 second. What are the values of *CPI* and *MIPS* for this performance experiment?

(b) What are the usual definitions of the terms *CISC* and *RISC* (reduced instruction set computer)? Identify two key architecture features that distinguish recent *RISC* and *CISC* machines.

2.[20%]

(a) A two-level memory (M1, M2) has the access times $T_{A1}=10^{-8}$ s and $T_{A2}=10^{-3}$ s. What must the hit ratio *H* be in order for the access efficiency to be at least 65% of its maximum possible value?

(b) Consider a cache with 64 blocks and a block size of 16 bytes. What block number does byte address 1200 map to?

3.[20%]

The available space list of a 16KB memory has the following entries at some time *t* :

Region hex address	*Size(bytes)*
0000	2K
1000	1K
2000	512
31FF	3K

The following sequence of allocation and de-allocation requests then occurs:

Time	*t+1*	*t+2*	*t+3*	*t+4*
Size of block to be allocated	1K	2K		1K
Address of block to be deallocated			2DFF	
Size of block to be deallocated			1K	

Determine the available space list after all these requests have been serviced using (a) best-fit and (b) first-fit allocation. Assume that the memory is searched in ascending address sequence.

4.[20%]

Define each of the following IO control methods: programmed IO, DMA controllers, IOPs (IO processor). List the advantages and disadvantages of each method with respect to program-design complexity, IO bandwidth, and interface hardware costs.

5.[20%]

(a) Show the steps of Booth's algorithm with negative numbers: 2 x -3 = -6, or 0010_2 x 1101_2= $1111,1010_2$.

(b) Explain briefly the Pipeline hazards? How can we resolve those problems?