國立臺北科技大學

九十三學年度機電整合研究所入學考試

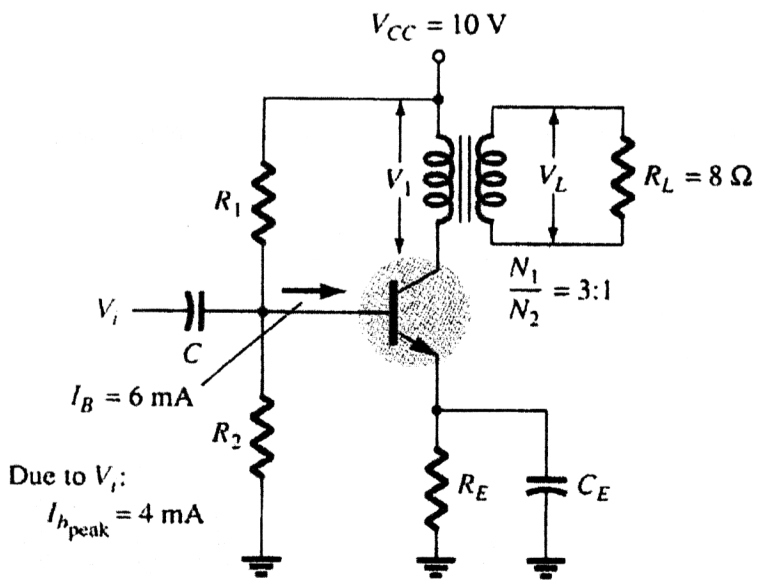
電子學試題

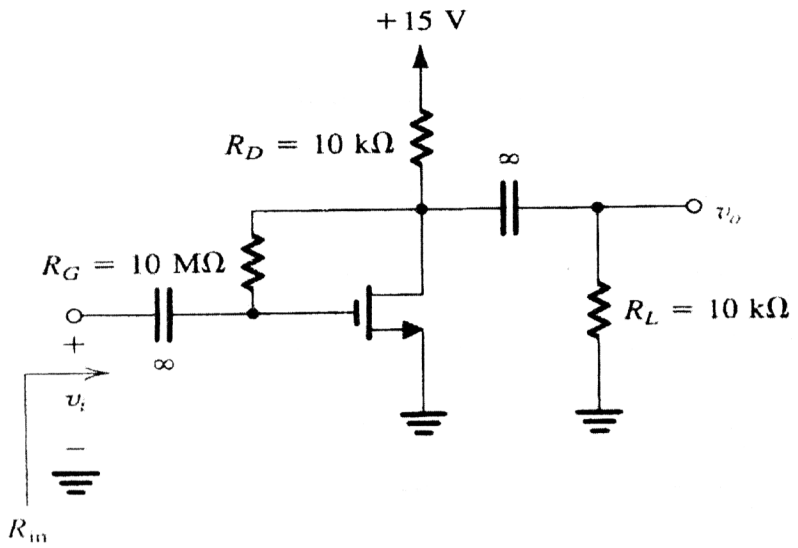
填准考證號碼

注意事項：

1. 本試題共 7 題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. Calculate the ac power delivered to 8-ohm speaker for the circuit. The circuit component values result in a dc base current of 6 mA, and the input signal (*Vi*) results in a peak base current swing of 4 mA. (20%)





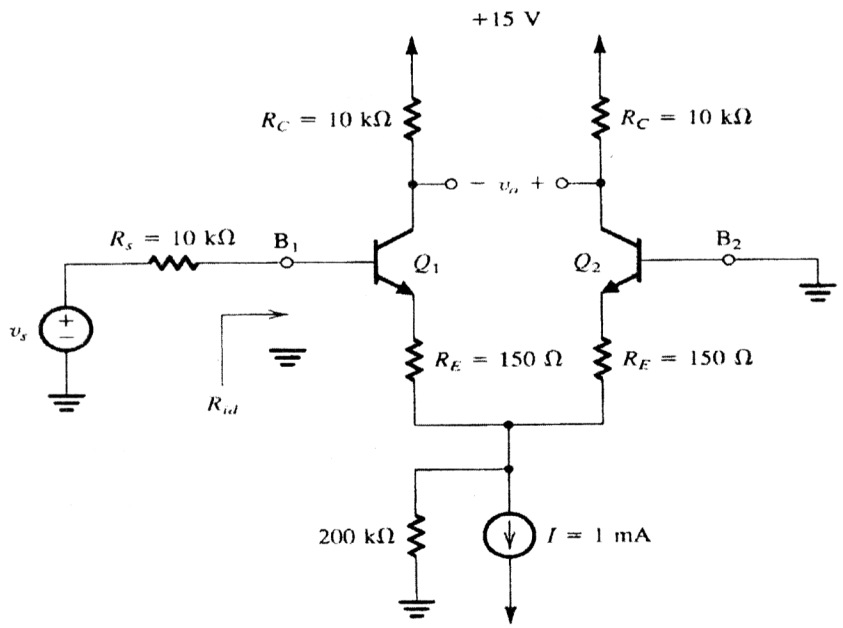
4. The differential amplifier uses transistors with b=100. Evaluate the following: (20%)

(a) The input differential resistance Rid.

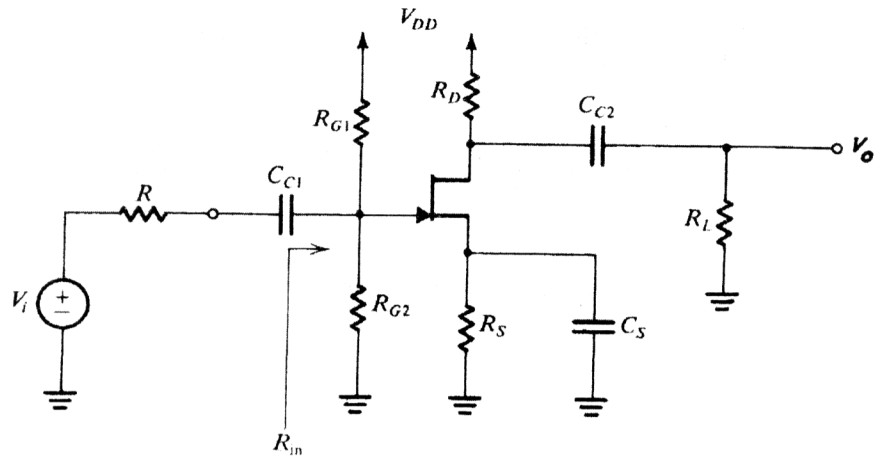
(b)The overall voltage gain v_o/v_s (neglect the effect of r_o).

(c)The worst case common-mode gain if the two collector resistances are accurate to within +- 1%.

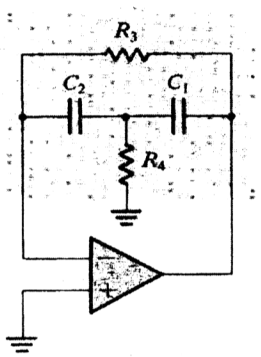
(d) The CMRR, in dB.



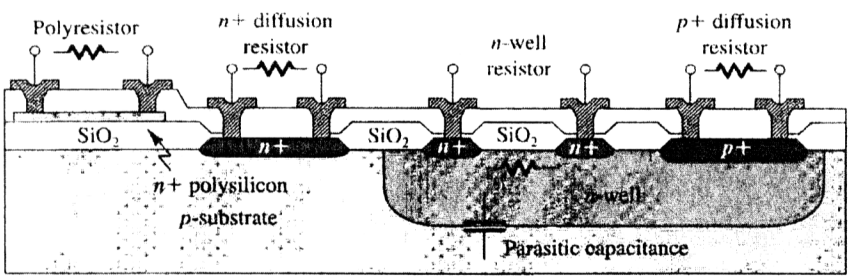
5. Select appropriate values for the coupling capacitors C_{C1} and C_{C2} and the bypass capacitor C_S of the amplifier, so that the low-frequency response will be dominated by a pole at 100KHz and that the nearest pole or zero will be at least a decade away. Let V_{DD} = 20V, R=100KΩ, R_{G1}=1.4Mohm, R_{G2} = 0.6MΩ, R_S = 3.5KΩ, R_D=5KΩ, r_o= infinite, R_L=10KΩ, Vp = -2V, and I_{Dss} = 8mA. Also, determine the midband gain. (15%)



6. Design the circuit to realize a pair of poles with $\omega_0 = 10^4$ rad/s and $Q = 1$. Select C_1=C_2=1 nF. (10%)



7. (a)Comapre various types of resistors available from a typical n-well CMOS process in terms of resistance per square. And why? (5%)



(a) Which type of capacitors available from a typical n-well CMOS process has better characteristic? And why? (5%)