國立臺北科技大學

九十三學年度電腦通訊與控制研究所入學考試

計算機結構試題

填准考證號碼

注意事項：

1. 本試題共 5 題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. [20%]

1) Does the following instruction set be fixed instruction format ? Why?

2) Please list the advantages of the fixed instruction format.

OPCODE	RD	RS1	RS2

OPCODE	DISP	RS2

OPCODE	RD	RS1

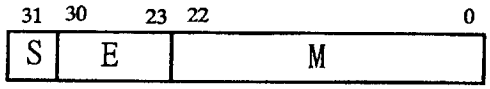
Instruction Set

2. [20%]

The number N represented by a 32-bit IEEE P754 standard floating-point number has the following set of interpretations.

If E=255 and M≠0, then N = NaN
If E=255 and M=0, then N = $(-1)^s \infty$
If 0<E<255, then N = $(-1)^s(2)^{E-127}$ (1.M)
If E=0 and M≠0, then N =$(-1)^s(2)^{-126}$ (0.M)
If E=0 and M=0, then N = $(-1)^s$ 0

1) find the internal representation of 6.25
2) Let A=25.5*2^{-75} and B=12.25*2^{60}, find the internal representation of A/B



3. [20%]

Suppose that a 2KB cache has set-associative address mapping. There are 16 sets, each containing four cache blocks (lines). The memory –address size is 32 bits, and the smallest addressable unit is the byte.

(a) To what set of the cache is the address $000010AF_{16}$ assigned?
(b) If the address $000010AF_{16}$ and $FFFF7xyz_{16}$ can be simultaneously assigned to the same cache set, what values can the address digits xyz have?

4. [20%]

Consider a pipelined processor with five stages: IF, ID, EX, MEM, and WB.

IF: Instruction Fetch
ID: Instruction Decode
EX: Execution/Effective address calculation

- Load/Store instruction : Effective address calculation
- ALU instruction : executing instruction
- Branch/Jump instruction: Condition decision

MEM: Memory operation/Branch instruction completion
WB: Write Back

A sample program is as follows:

I_1: R1 ← 4 **(load instruction)**
I_2: R2 ← 6 **(load instruction)**
I_3: R_3 ← R1 – R2
I_4 : **if** R_1 = 0 **then go to L**
I_5: R1 ← C
I_6: R3 ← B
I_7 : **L:**R6 ← R1 + R2
I_8 : R_2 ← R3

1) Please find the pipeline speedup (**Note**: Internal forwarding technique is employed)
2) Repeat 1) after executing delay branch.

5. [20%]

Answer the following questions:

1) What is the difference between Mealy type and Moore type finite-state machine?
2) Is pipeline needed to handle WAR (Write After Read) hazard? Why?
3) For any number A and B, assuming the execution time of A*B is T. Does T be constant for booth algorithm?
4) Can PCI system bus be replaced with USB 2.0? Why?
5) When the length of horizontal and vertical microinstructions should be equal?