國立臺北科技大學

九十三學年度電機工程系碩士班入學考試

計算機組織試題

填准考證號碼

注意事項：

1. 本試題共 10 題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. (10%) What is the major difference between the implementation of control logic for the single-cycle processor implementation and the multi-cycle implementation?

2. (5%) Consider a cache-based memory system. The cache miss penalty is 5 clock cycles, and all instructions normally take 10 clock cycles (ignoring memory stalls). Assume the miss rate is 12%, and there is an average of 3.0 memory references per instruction. What is the impact on performance when behavior of the cache is included?

3. (10%) Consider a system containing a 128K-byte cache. Suppose that set-associative mapping is used in the cache, and that there are four sets each containing 4K cache pages. The physical address size is 32 bits, and the smallest addressable unit is the byte. Design the cache structure, and show how the physical addresses are interpreted?

4. (10%) Draw an 8×8 butterfly network.

5. (5%) Show the hardware to be used for the addition and subtraction of two binary numbers in signed-2's complement representation. (5%) Indicate how an overflow is detected.

6. (10%) Draw the circuit of a 5 by 32 decoder constructed with four 3 by 8 decoders (with enable inputs) and one 2 by 4 decoder.

7. (10%) For the RISC design, draw the execution diagram for the following RISC program (with the contents of R1 nonzero after the subtraction), and indicate any data or control hazards that are present:

1. SUB R1, R1, R2
2. BNZ R1, 000E
3. AND R3, R1
4. OR R3, R1

8. Explain the following terms.

(a) (3%) control word

(b) (3%) control memory

(c) (3%) microinstruction

(d) (3%) microprogram

(e) (3%) microoperation

9. (10%) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following arithmetic operations in conjunction with carry C_{in}:

S	C_{in}=0	C_{in}=1
0	$F = A + B$	$F = A + 1$
1	$F = A - 1$	$F = A + \overline{B} + 1$

Show the logic diagram of two least significant stages.

10. (10%) What is the difference between an immediate, a direct, and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?