國 立 臺 北 科 技 大 學

九十二學年度電腦通訊與控制研究所入學考試

電子學（丁組）試題

注意事項：

1. 本試題共【9】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

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1. The voltage regulator is to power a car radio at $V_L = 9$ V from an automobile battery whose voltage may vary between 11 and 13.6 V. The current in the radio will vary between 0 (off) to 100 mA (full volume). The equivalent circuit is shown in Fig. 1.

   (a) Find the maximum Zener diode current. (5%)

   (b) The value of the current-limiting resistor R_X. (5%)

2. In the circuit shown in Fig. 2, V_{BB} is set equal to these values:

   (a) $V_{BB} = 0.5$ V.　(b) $V_{BB} = 1.5$ V.　(c) $V_{BB} = 3$ V.

   Determine the state of the transistor for each value of the base supply voltage.
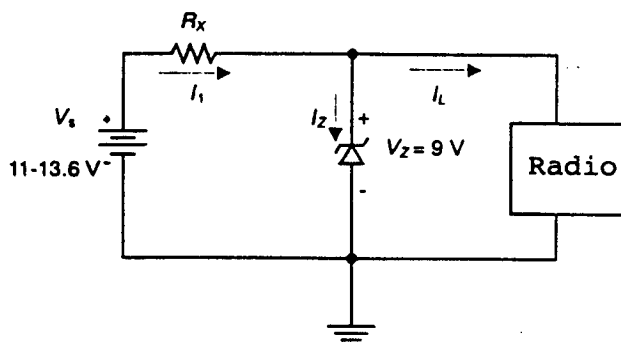
   Assume V_{BE} (on) = 0.7 V. (15%)
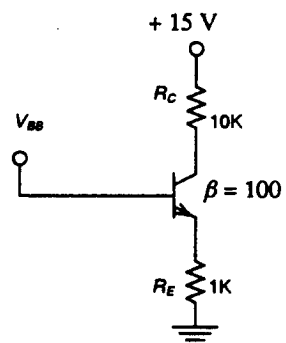

Fig. 1 Circuit for problem 1　　　　Fig. 2 Circuit for problem 2

3. For the circuit in Fig. 3, find the differential-mode gain. (10%)
   Assume $V_{BE}(\text{on}) = 0.7$ V and $\beta = 100$ for Q_1 and Q_2.

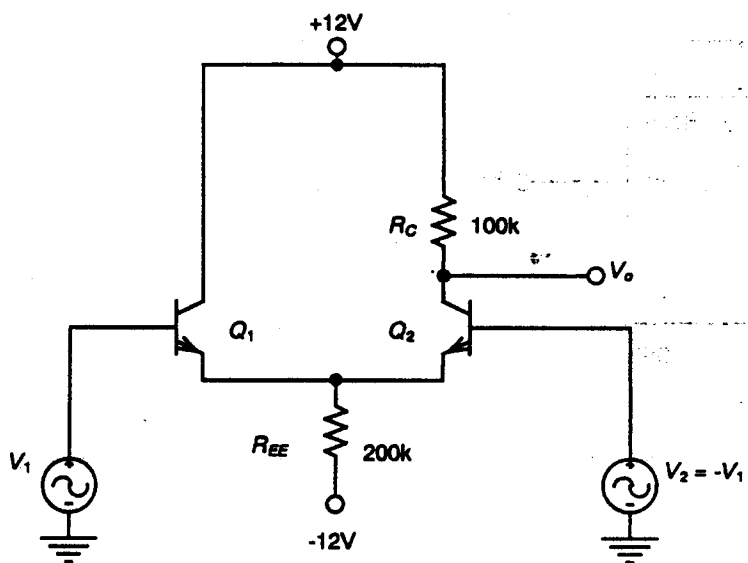4. Find the output voltage V_o for the circuit in Fig. 4. (10%)
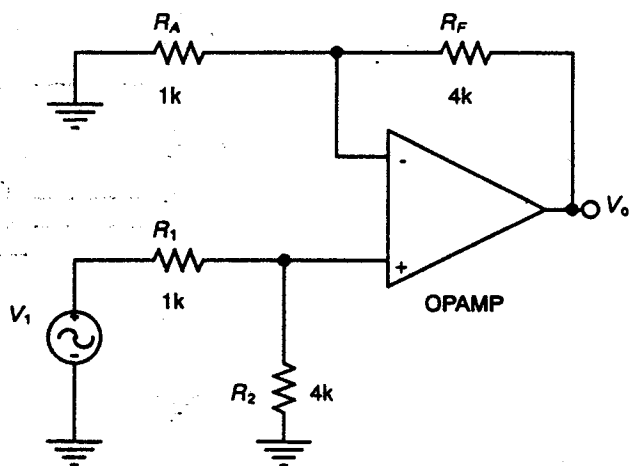

Fig. 3 Circuit for problem 3

Fig. 4 Circuit for problem 4

5. Consider a two-pole active filter, as shown in Fig. 5. Derive the expression for the transfer
   function $T(s) = \dfrac{V_o(s)}{V_i(s)}$, where $s = j\omega$. (20%)
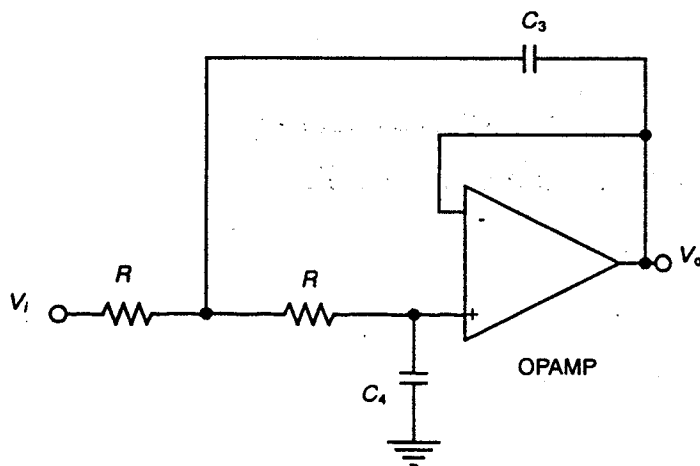

Fig. 5 Circuit for problem 5

6. Consider the circuit in Fig. 6. Design the R_A and R_B in the circuit such that the frequency is 50 KHz and the duty cycle is 75 percent. Let $C = 1$ nF. (10%)
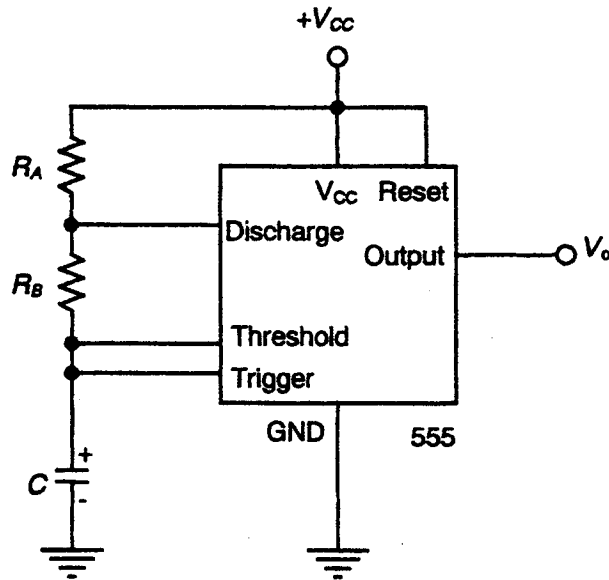

Fig. 6 Circuit for problem 6

7. Implement the logic function $Y = AB + C(D + E)$ in a CMOS design. The signals A, B, C, D, and E are available. (10%)

8. A 4M-bit memory chip is partitioned into 32 blocks with each block having 1024 rows and 128 columns. Give the number of bits required for the row address, column address, and block address. (6%)

9. (a) Sketch a static memory cell in CMOS technology. (5%)
   (b) Sketch the one-transistor dynamic RAM cell. (4%)