國立臺北科技大學

九十二學年度電機工程系碩士班入學考試

計算機組織試題

填准考證號碼

注意事項：

1. 本試題共【11】題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. Answer the following questions about pipeline design
   (a) (5%) What is control hazard? Give a simple example to explain it.
   (b) (5%) How to overcome control hazard? Give a simple example to explain it.

2. (7%) Suppose you have a 2Kx8 bits ROM . Show how you can use it as a 4Kx4 bits ROM.

3. Consider a computer with a physical address space of 24 bits and a 8-bit data bus. The main memory (byte addressable) has the following organization:
   - Addresses 0 to 65535 are occupied by the BIOS.
   - The RAM is mapped into the range 0x200000 to 0x3FFFFF
   - The size of the video memory is 64K bytes beginning at address 0xF00000

   (a) (3%) What is the size of the RAM memory (in bytes)?
   (b) (5%) Draw the address decode logic necessary to select each one of the three ranges of memory (full address decoding). Assume further that each type of memory (BIOS, RAM and VIDEO) is implemented using a single chip.

4. (5%) What are interrupts? How do they increase system performance?

5. (a) (2%) A machine has a 16-bit byte addressable virtual address space. The page size is 1Kbyte. How many pages of virtual address space exist?

(b) (2%) The logical address space in a computer system consists of 64 segments. Each segment can have up to 64 pages of 1K words in each. Physical memory consists of 4K blocks of 1K words each. Show the format of logical and physical address formats.

(c) (6%) A virtual memory has a page size of 1024 words, eight virtual pages and four physical page frames. The page table is as follows:

Virtual Page	Page Frame
0	not in memory
1	not in memory
2	3
3	1
4	not in memory
5	0
6	2
7	not in memory

- Make a list of all virtual addresses that will cause page faults.
- What are the physical addresses for 0, 3728, 1023,1024,5121,7800, and 6144?

(d) (10%) A computer has 16 pages of virtual address space but only four page frames. Initially, the memory is empty. A program references the virtual pages in the order: 0, 7, 2, 7, 5, 8, 9, 2, 4

- Which references cause a page fault with LRU? Show the contents of main memory after each program reference is serviced.
- Which references cause a page fault with FIFO? Show the contents of main memory after each program reference is serviced.

6. (a) (5%) Design a pipelined hardware to perform the following operation:

$$x(i) = A(i) + B(i) \times C(i), \quad i = 1,\ldots,n$$

(b) (5%) Please make a comparison between the proposed pipelined hardware and nonpipeline hardware.

注意：背面尚有試題

7. (5%) A 2-line to 4-line decoder has "address-lines" A and B which select the desired input; "B" is the LSB; The outputs are labeled EN0, EN1, EN2, and EN3, with EN0 true when both address-lines are false. Write the Boolean equations for this decoder. Draw the logic diagram using AND, OR and NOT gates.

8. (5%) A PCI bus is operating with a 66Mhz clock and a 32-bit wide bus. Assuming that arbitration and other setup requires 4 bus cycles, how long does it take to transfer 1K bytes of data? What is the data rate of this transfer in Mbytes/sec?

9. (10%) Please describe the following terminologies
   (a) Amdahl's Law
   (b) MFLOPS
   (c) VLIW
   (d) Micro code
   (e) RISC processor

10. An interface unit has two handshake lines: an input line labeled STB(strobe), and an output line labeled IBF(Input Buffer Full). A low signal on STB loads data from the bus to an interface register. A high signal on IBF indicates that the data have been accepted by the interface. IBF goes low after an I/O read signal from the CPU.
   (a) (5%) Draw a block diagram showing the pertinent interconnections between the CPU, the interface, and the I/O device.
   (b) (5%) Draw a timing diagram for the handshake transfer.

11. Assume that we have a processor running at 100 MHz and that the processor has the following instruction set definition:

Type of instructions	# of cycles	Weight
Memory Access (Load and Store)	3	0.3
Integer Arithmetic	2	0.3
Logic Operations (AND, OR, XOR, etc)	1	0.2
Floating-point Arithmetic	8	0.1
Jump and Branch	3	0.1

   (a) (5%) What is the CPI for this processor?
   (b) (5%) What is the MIPS rate of this processor?