國立臺北科技大學 102 學年度碩士班招生考試

系所組別：2240 電腦與通訊研究所丁組

第一節　數位邏輯設計　試題

注意事項：

1. 本試題共 6 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Perform each of the following conversions.
   (a) $(511)_{10} = (\_\_\_\_\_)_8$ (5%)
   (b) $(110010011)_2 = (\_\_\_\_\_)_{BCD}$ (5%)
   (c) $(1C8)_{16} + (270)_8 = (\_\_\_\_\_)_{10}$ (5%)

2. In an audio CD, the audio voltage signal is typically sampled about 44,000 times per second, and the value of each sample is recorded on the CD surface as a binary number. In other words, each recorded binary number represents a single voltage point on the audio signal waveform.
   (a) If the binary numbers are six bits in length, how many different voltage values can be represented by a single binary numbers? (5%)
   (b) If eight-bit numbers are used, how many bits will be recorded on the CD in 8 seconds? (5%)
   (c) If a CD can typically store 6 billon bits, how many seconds of audio can be recorded when ten-bit numbers are used? (5%)

3. A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3, A_2, A_1, and A_0 represent the individual bits with A_0 equal to the LSB. Please design a logic circuit that will produce a HIGH output (F) whenever the binary number is greater than 0010 and less than 1000. (10%)

4. Please design a multiplier circuit that takes two-bit binary numbers x_1x_0 and y_1y_0 and produces an output binary number $z_3z_2z_1z_0$ that is equal to the arithmetic product of the two input numbers. Design the logic circuit for the multiplier. (20%)

5. A sequential network contains a register of four flip-flops. Initially a binary number N ($0000 \le N \le 1001$) is stored in the flip-flops. After a single input pulse is applied to the network, the register should contain $N + 0101$. In other words, the function of the sequential network is to add 5 to the contents of a 4-bit register. Design the network using four J-K flip-flops (A, B, C, D flip-flops and D is the LSB flip-flop). (20%)

6. Figure 1(a) is a diagram of a typical stepper motor with four coils. A synchronous counter supplies the appropriate sequential outputs to drive a stepper motor. Since this stepper motor can rotate either clockwise (CW) or counter clockwise (CCW), we have a Direction input, D, which is used to control the direction of rotation. The state diagrams in Figure 1(b) show the two cases. For CW rotation to occur, we must have D = 0, and the state of the counter, BA, must follow the sequence 11, 10, 00, 01, 11, 10, …. ,and so on, as it is clocked by the Step input signal. For CCW rotation, D = 1, and the counter must follow the sequence 11, 01, 00, 10, 11, 01, ..., and so on.
   (a) Show the circuit excitation table for Figure 1(b). (10%)
   (b) Design this synchronous counter using two J-K flip-flops (B, A flip-flops and A is the LSB flip-flop) and simple logic gates. (10%)

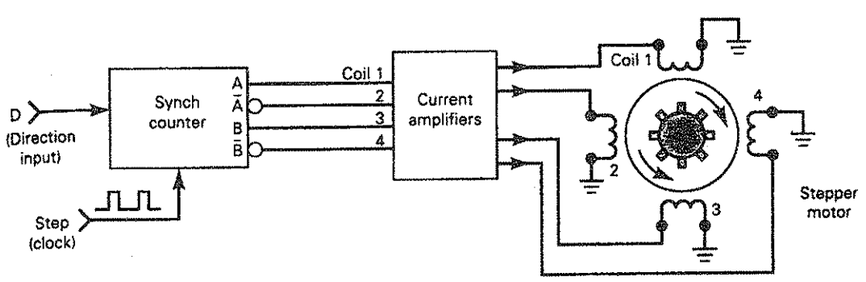

Figure 1(a) A synchronous counter supplies the appropriate sequential outputs to drive a stepper motor.

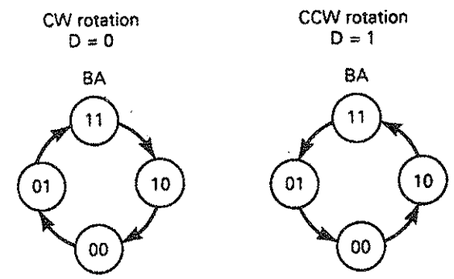

Figure 1(b) State transition diagrams for both states of Direction input, D.