國立臺北科技大學 101 學年度碩士班招生考試

系所組別：1521 自動化科技研究所乙組

第二節　電子學　試題（選考）

注意事項：

1. 本試題共五題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. A full-wave rectifier circuit with 2-kΩ load operates from a 120V (rms) 60Hz household supply through a 5-to-1 transformer having a center-tapped secondary winding. It uses two silicon diodes that can be used to model to have a 0.7V drop for all currents. (24pts, each sub-problem is 6 pts)
   (a) What is the peak voltage of the rectified output?
   (b) For what fraction of a cycle does each diode conduct?
   (c) What is the average output voltage?
   (d) What is the average current in the load?

2. For each of the circuits shown in Figure 1, find the emitter, base, and collector voltages and currents. Use β=30, but assume $|V_{BE}|$= 0.7 V independent of current level. (24 pts, each sub-problem is 6pts)

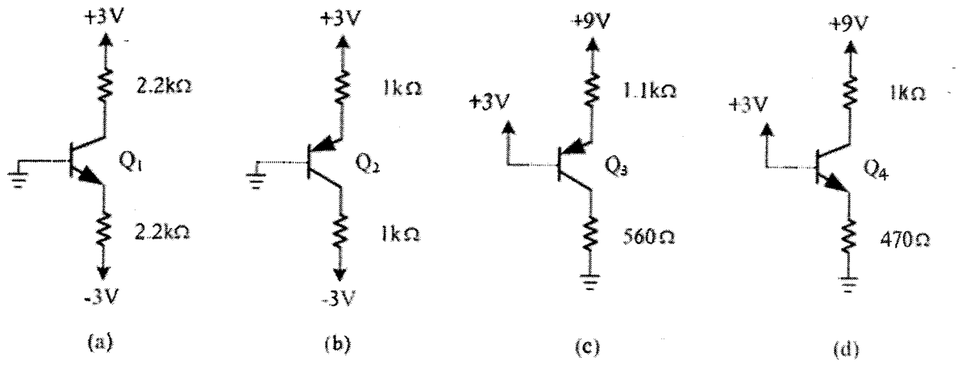

Figure 1

3. See Figure 2 and assume that $R_1C_1 >> R_2C_2$. (24 pts, each sub-problem is 8pts)
   (a) Derive the transfer function of the circuit.
   (b) Sketch the Bode plot for the magnitude response of the circuit.
   (c) Design a circuit to provide a gain of 60dB in the ``middle frequency range,'' a low-frequency 3-dB point at 100Hz, a high-frequency 3-dB point at 10kHz, and an input resistance (at high frequency) of 1kΩ.

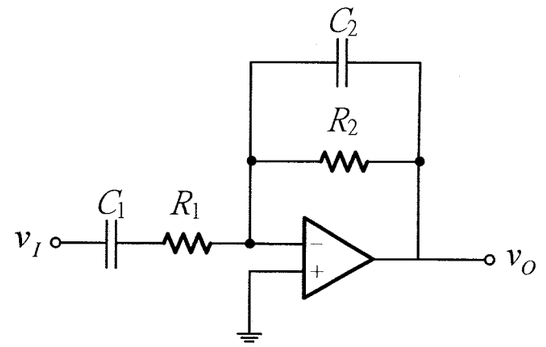

Figure 2

4. The differential amplifier circuit shown in Figure 3 utilizes a resistor connected to the negative power supply to establish the bias current I. (16 pts, each sub-problem is 4 pts)
   (a)For $v_{B1} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where v_{id} is a small signal with zero average, find the magnitude of the differential gain, $|v_O/v_{id}|$.
   (b) For $v_{B1} = v_{B2} = v_{icm}$, find the magnitude of the common-mode gain, $|v_O/v_{icm}|$.
   (c) Calculate the CMRR.
   (d) If $v_{B1} = 0.1\sin(2\pi \cdot 60t) + 0.005\sin(2\pi \cdot 1000t)$ volts,
   $v_{B2} = 0.1\sin(2\pi \cdot 60t) - 0.005\sin(2\pi \cdot 1000t)$ volts, find v_O.

注意：背面尚有試題

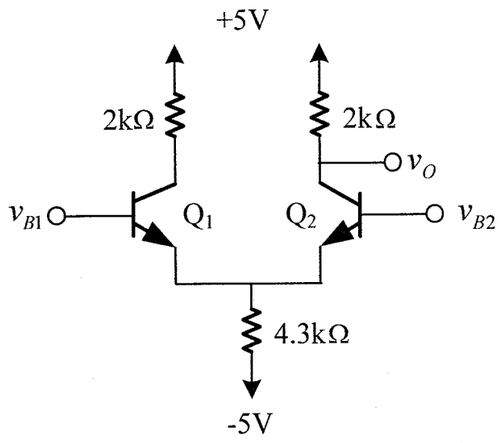

Figure 3

5. A logic-circuit family intended for use in a digital-signal-processing application in a newly developed hearing aid can operate down to single-cell supply voltages of 1.2V. If for its inverter, the output signals swing between 0 and V_{DD}, the ``gain-of-one'' points are separated by less than $1/3V_{DD}$, and the noise margins are within 30% of one another, what ranges of values of (a) V_{IL}, (b) V_{IH}, (c) V_{OL}, (d) V_{OH}, (e) NM_L, and (f) NM_H can you expect for the lowest possible battery supply? (12 pts, each sub-problem is 2 pts)