國立臺北科技大學

100學年度研究所碩士在職專班入學考試

電腦與通訊研究所

丁組：電子學試題

填准考證號碼

注意事項：

1. 本試題共四題，配分共 100 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。

一、 Consider the design of a CMOS exclusive or gate.

1. Write the logic function of an exclusive or gate with input A and B.(5%)
2. Design and sketch the exclusive or gate by means of NAND gates. (5%)
3. Simplify the below logic function. (5%)

$$Y = BC + AB(\overline{C} + D) + AD(\overline{B} + BC) + BC(A + \overline{D}) + B(A\overline{C} + \overline{A}CD)$$

4. Design and sketch the above logic function by means of NAND gates. (5%)

二、 Please design the requested circuit and sketch the schematic:

1. Use NAND gates, resistors and capacitors to design a power-on-reset circuit. (10%)
2. Use op-amps and resistors to design an instrumentation amplifier with 40dB voltage gain. (10%)
3. Use capacitors and diodes to design a voltage doubler. (10%)

三、 Fig.1 shows an output stage of a CMOS op-amp, where V_{DD} = 5V , V_{Bias}=2.5V and C_L = 1nF. Please use these parameters of MOS $|V_{TN}| = |V_{TP}| = 0.7V$, $\beta_n = \beta_p = 100\mu A/V^2$ and V_A=100V of MOS to calculate the following questions.

$\beta = \mu C_{ox}\frac{W}{L}$.

1. Calculate the input "trip point", which means that the input voltage starts to make V_{out} change sharply. (10%)
2. Calculate the small signal gain $Av = v_o/v_{in}$ when operating at the trip point. (10%)
3. Calculate the negative slew rate when v_o decreases from high to low. (5%)

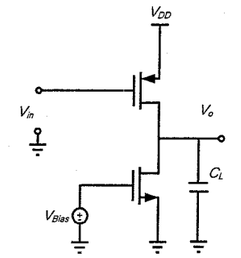

Fig.1

四、 According to the active filter shown in Fig.2, please answer the following questions:

1. Find the DC gain of V_o/V_{in}. (5%)
2. Find the transfer function of the voltage gain. (5%)
3. Find the input impedance. (5%)
4. Sketch its magnitude frequency-response characteristics. (5%)
5. Sketch its phase frequency-response characteristics. (5%)

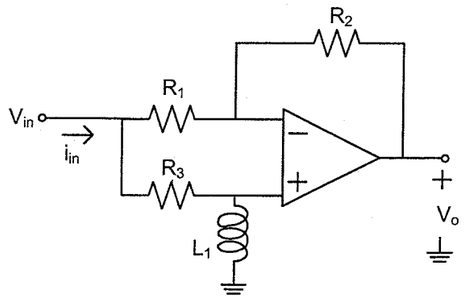

Fig.2