國立臺北科技大學 102 學年度碩士班招生考試

系所組別：2230 電腦與通訊研究所丙組

第二節　電子學　試題

注意事項：

1. 本試題共五題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Please calculate the input impedance (Z_{in}) of the diode-connected PMOS as shown in Fig. 1. Assume no body effect exists in the device. **(10%)**

2. Figure 2 shows a layout of a CMOS logic circuit.

(a) Sketch the schematic of Fig. 2, where ***a*** and ***b*** are the inputs, and ***out*** is the output **(5%)**

(b) What is the logic function in Fig. 2? **(5%)**

(c) Why NAND gate is preferably used in CMOS logic circuits as compared with NOR gate for the consideration of package density? **(10%)**

(d) Design the logic function $Y = \overline{A}B + A\overline{B}$ using NAND gates. **(10%)**

3. In the Fig. 3, the op-amp circuit has three internal critical frequencies as follow: 1.2KHz, 50KHz, and 250KHz. If the midrange open-loop gain is 100dB, is the amplifier configuration stable, marginally stable, or unstable? **(15%)**

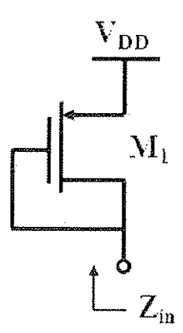

Fig. 1

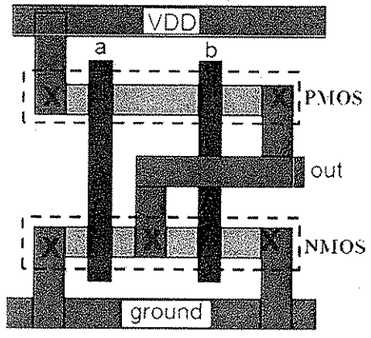

Fig. 2

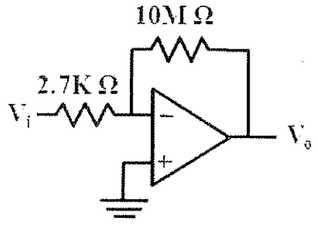

Fig. 3

4. For the circuit shown in Fig.4, let $V_{BE(on)}$=0.7V, β=100, and $V_{CE(sat)}$=0.2V.

(a) Determine the *Q*-point of the circuit. **(10%)**

(b) Plot the load line and indicate the *Q*-point on the collector current-voltage characteristic plot. Indicate important data and the associated units on the plot. **(10%)**

5. Fig. 5 shows a feedback circuit. Please find:

(a) The feedback topology? **(5%)**　**(b)** $|\beta A|$ **(5%)**

(c) V_o/V_s **(5%)**　**(d)** R_{out} **(5%)**　**(e)** R_{in} **(5%)**

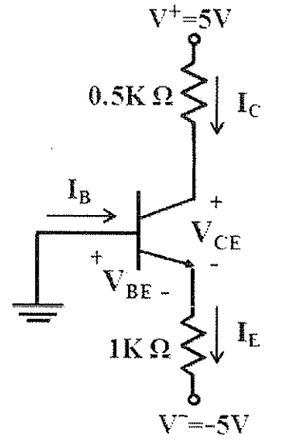

Fig. 4

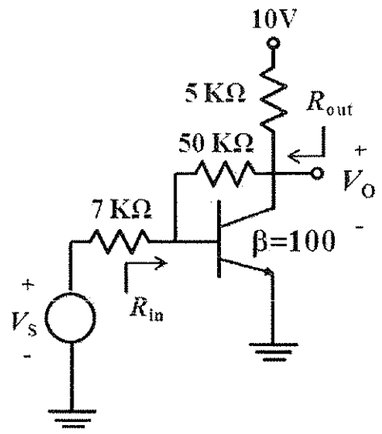

Fig. 5