國立臺北科技大學

九十九學年度研究所碩士在職專班入學考試

電腦與通訊研究所

甲組：計算機結構試題

填准考證號碼

注意事項：

1. 本試題共【4】題，配分共 **100** 分。
2. 請按順序標明題號作答，不必抄題。
3. 全部答案均須答在試卷答案欄內，否則不予計分。

1. In multiprogramming environment, more than one program could be executed concurrently. Describe the main features of the following schemes: (**32**%)
   (a) *paging*, (b) *demand paging*, and (c) *demand segmentation*, respectively, used for multiprogramming. (**8**% each)
   (d) State the impact of *thrashing* on a multiprogramming system. (**8**%)

2. Assume that a memory system used a **225**-MHz clock. The memory transmitted a **7**-word data at the rate of **1** word per cycle, and the word size is **4** bytes. (**24**%)
   For *read* from memory, the accesses occur as following steps.
   Step-1: **1** cycle to accept the address,
   Step-2: **2** cycles of latency, and
   Step-3: **7** clock cycles to read a 7-word data.
   For *write* to memory, the accesses occur as following step.
   Step-1: **1** cycle to accept the address,
   Step-2: **2** cycles of latency,
   Step-3: **7** clock cycles to write a 7-word data, and
   Step-4: **4** cycles to recover and write the error correction code.
   Calculate the *maximum data bandwidth* in megabytes per second (MBps) for the following different access patterns, *P*1 to *P*3, respectively.
   (a) *P*1: All *reads* to memory. (**8**%)
   (b) *P*2: All *writes* from memory. (**8**%)
   (c) *P*3: A mix of **70**% *reads* from memory and **30**% *writes* to memory. (**8**%)

3. Some computer contained a cache, main memory, and a hard disk used for virtual memory. If a referenced word is in the cache, system takes **40** ns to access it. If the word is in main memory but not in the cache, system takes **160** ns to load it to the cache, and then starts the reference again. If it is not in memory, system takes **1.06** ms to fetch it from the hard disk, followed by **160** ns to copy it to the cache, and then starts the reference again.
   Suppose that the cache hit ratio is **0.75**, and the main-memory hit ratio is **0.6**. Calculate the *average time* (in microsecond) required to access a referenced word on this system. (**20**%)

4. Let a nonpipelined processor have a clock rate of **3.0** GHz and an average CPI (cycles per instruction) of **4**. An upgrade to processor introduces a **5**-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor must be reduced to **2.48** GHz. (**24**%)
   (a) What is the speedup achieved for a typical program with **100** instructions to be processed. (**8**%)
   (b) What is the MIPS rate for each processor? (**8**%, **8**%)