國立臺北科技大學九十六學年度碩士班招生考試

系所組別：1522 自動化科技研究所乙組

第二節 計算機概論（選考）試題

注意事項：

1. 本試題共 6 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1.(40%) Please explain: (each 4%)

(1) RISC
(2) OSI
(3) RTOS
(4) SoC
(5) Firewall
(6) WLAN
(7) Semaphore
(8) URL
(9) CDMA
(10)What is the difference between "compiler" and "interpreter"?

2.(1)(5%) What is the object-oriented programming?

(2) (5%) Briefly explain three main concepts supported by a general object-oriented programming language?

3.Consider a computer equipped with 2M Bytes main memory and 128K Bytes cache, and the size of each block is assigned as 64 Bytes. Please depict the arrangement of address bits (thus, tag bits, block/set bits, displacement/offset bits) for the following conditions.

(1)(5%)Direct-mapped cache
(2)(5%)Fully associative-mapped cache
(3)(5%)4-way set associative-mapped cache (thus, each set has 4 blocks)

4.(1)(5%) What is the biased single precision IEEE 754 floating point format of 0.9375?

(2)(5%) What is the purpose to bias the exponent of the floating point numbers?

5.The terms big-endian and little-endian were originally found in Jonathan Swift's book, Gulliver's Travels. Now all processors must be designed as either big-endian or little-endian. For example, Intel 80x86 is little-endian and Motorola 680x0 is big-endian.

(1) (5%)Explain the different between big-endian and little-endian.
(2) (5%)Please illustrate big-endian and little-endian by considering the number 4097 stored in a 4-byte integer.

Address	Big-endian representation	Little-endian representation
00		
01		
03		
04		

6.Given three classes of instructions: class A, B, and C, having CPI_A=a, CPI_B=b, and CPI_C=c, where CPI stands for cycles per instruction.

(1)(5%) If we can tune the clock rate to 120% without affecting any $CPI_{A,B,C}$, what is the performance gain G(a)=[$performance_{now}$/ $performance_{original}$-1]?

(2)(5%) Increasing clock rate to 150% and then $CPI_{A'}$=1.5 CPI_A, while $CPI_{B'}$ and $CPI_{C'}$ remain unchanged. If class A instructions account for 40% of all dynamic instructions, what is the performance gain G(b)?

(3)(5%) Now let the compiler come into play. Given original clock rate, if for every class A instruction to be eliminated, there must be *x* class B instructions and *y* class C instructions added into the execution stream. Under what condition would you want to eliminate class A instructions?