at 5-1

國立臺北科技大學

九十四學年度自動化科技研究所入學考試

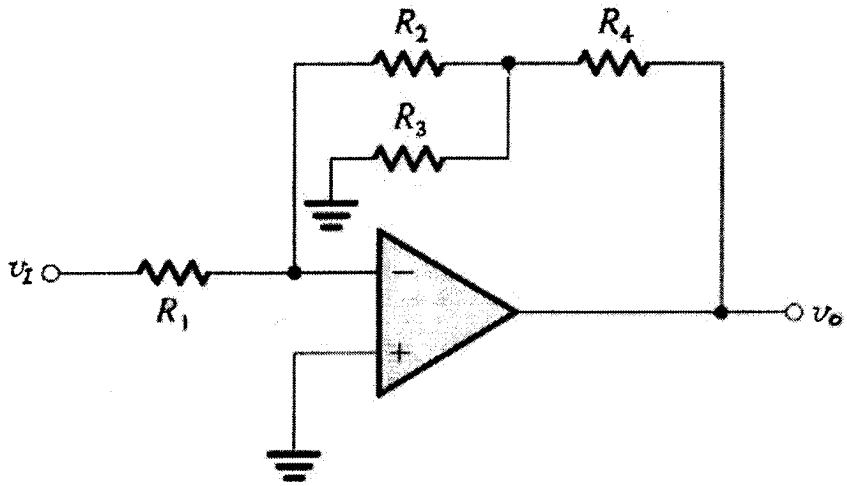
電子學試題

填准考證號碼

注意事項：

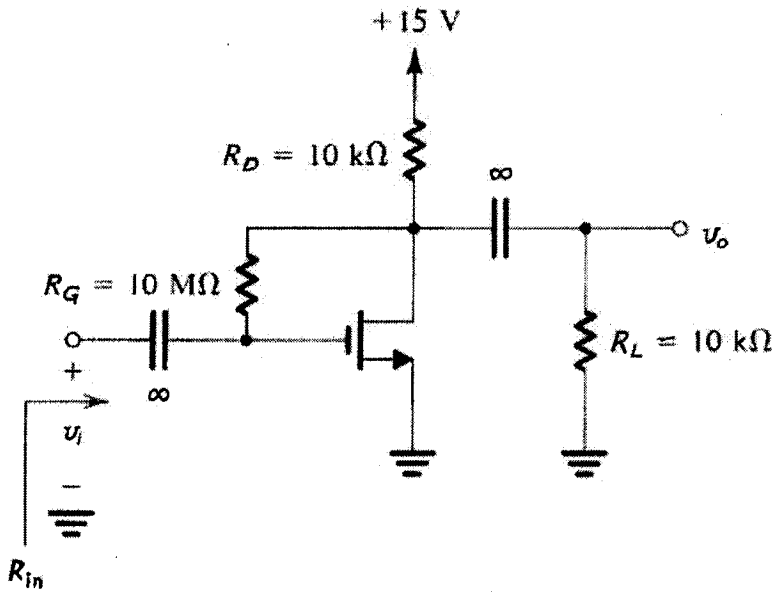
1. 本試題共五題，配分共 100 分。
2. 請按順序標明題號作答，並列出相關計算過程，不必抄題。
3. 計算題的部份，最後之答案請劃上底線並標示其單位。
4. 全部答案均須答在答案卷之答案欄內，否則不予計分。

1. For the circuit shown below,
   (a) Derive an expression for the gain v_O / v_I (10%)
   (b) Find the voltage gain, for R_1= 10 kΩ, R_2= 20 kΩ, R_3= 30kΩ, R_4= 60kΩ. (5%)
   (Assume that the op amp is ideal.)



2. For the circuit shown below, derive its
   (a) small-signal voltage gain (10%)
   (b) input resistance (10%)

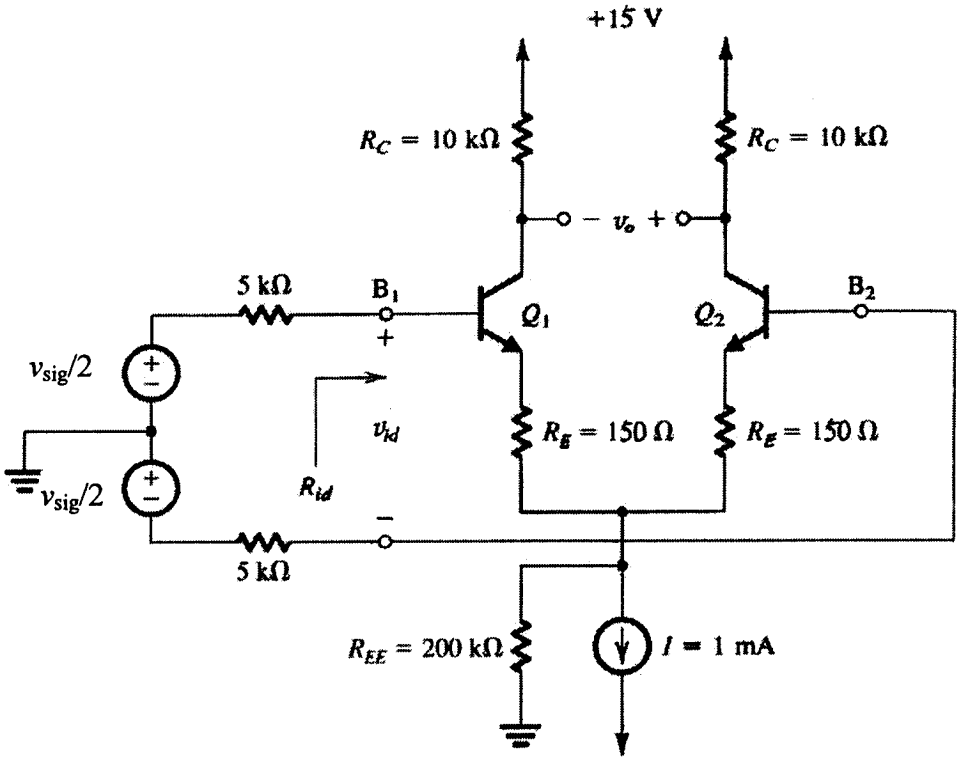
   The transistor has V_t=1.5V, $K_n'(W/L)$=0.25 mA/V^2, and V_A=50V.



3. Sketch the high frequency hybrid π model of the BJT and clearly describe the circuit parameters in the model. (15%)

注意：背面尚有試題

4. For the circuit shown below, evaluate the following (β=100) :　(25%)
   (a) The input differential resistance R_{id}.
   (b) The overall differential voltage gain v_o/v_{sig} (neglect the effect of r_o)
   (c) The worst-case common-mode gain if the two collector resistances are accurate to within ±1%.
   (d) The CMRR, in dB.
   (e) The input common-mode resistance (assuming that the Early voltage V_A =100V).



5. 如下圖之接線，訊號產生器輸出載波訊號 $v_{carrier}$，請設計一電路(圖中之電路 A)將此載波訊號注入單相交流 110V 家用電源線插座內。
   (a) 請將相關電路繪出 (10%)
   (b) 說明你的設計理念，以及設計時需注意哪些地方。(15%)

   $v_{carrier} = 7\sin(400000\pi t)$ (V)