國立臺北科技大學 100 學年度碩士班招生考試

系所組別：2240 電腦與通訊研究所丁組

第一節　數位邏輯設計　試題

注意事項：

1.本試題共 8 題，配分共 100 分。
2.請標明大題、子題編號作答，不必抄題。
3.全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. A typical personal computer uses a 16-bit address code for its memory locations. Please answer the following questions:
   (a) What is the range of addresses? 5 分
   (b) What is the total number of memory locations? 5 分

2. Apply the input waveforms of Figure 1 to an Exclusive-OR (XOR) gate, and draw the output waveform. 10 分

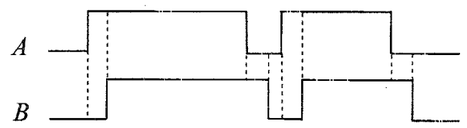


Figure 1　Input waveforms

3. Design a logic circuit with three inputs *A*, *B*, *C* and an output *Y* that goes LOW only when *A* is LOW while *B* and *C* are different. 10 分

4. Construct a MOD-13 ripple counter by *J-K* Flip-Flops that will count from 0000 (zero) through 1100 (decimal 12). 10 分

5. A state table for the PRESENT and NEXT states of the three *J-K* Flip-Flops *C*, *B*, and *A* is shown in Table 1. Please answer the following questions.
   (a) Use the state table, Table 1, to set up a state transition diagram. 10 分
   (b) Use the state table, Table 1, to implement the synchronous counter circuits by the three *J-K* Flip-Flops and some combinational logics. 20 分

Table 1　State table

PRESENT State			NEXT State		
C	*B*	*A*	*C*	*B*	*A*
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0

6. Construct a *Switch Circuit* as shown in Figure 2 by combinational logics which function describes in the following: 10 分
   (1) If *control* = 0, then *X* = *A* and *Y* = *B*,
   (2) If *control* = 1, then *X* = *B* and *Y* = *A*.

7. Use 8-to-1 multiplexer to implement a logic function described by the truth table, shown in Table 2. 10 分

8. Use hardware description language (For example, VHDL or Verilog) to implement a 4-to-2 *Encoder*, which function block and truth table are shown in Figure 3. 10 分

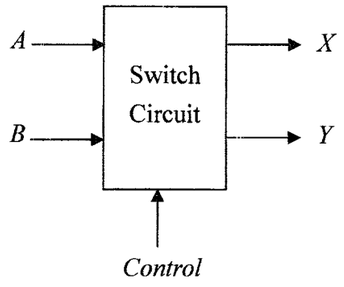
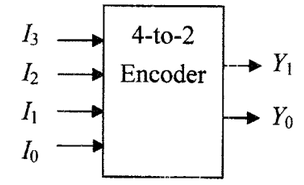


Figure 2　Switch circuit

Table 2　Truth table

Input			Output
C	*B*	*A*	*Y*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



(a) Function block

Input				Output	
I_3	I_2	I_1	I_0	Y_1	Y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

(b) Truth table

Figure 3　4-to-2 Encoder