國立臺北科技大學 100 學年度碩士班招生考試

系所組別：2210 電腦與通訊研究所甲組

第二節　計算機結構　試題

注意事項：

1. 本試題共【10】題，配分共【100】分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. What are the *four* main components of any general-purpose computer? (6%)

2. What is the distinction between *temporal locality* and *spatial locality*? (6%)

3 What is the difference between *SRAM* and *DRAM* in terms of application? (6%)

4. List *three* techniques for performing I/O in a computer? (6%)

5. Are *all of the pages* of a process necessary to be loaded in main memory completely while the process is executing? Why? (6%)

6. What is the difference between a *hardware pipeline* and a *software pipeline*? (10%)

7. What is the distinction between *horizontal* and *vertical microinstructions*? (10%)

8. Consider a 32-bit microprocessor whose bus cycle is the same duration as that of a 16-bit microprocessor. Assume that, on average, ***x***% of the instructions and operands are **32** bits long, ***y***% are **16** bits long, and *z*% are only **8** bits long, where $x + y + z = 100$. Derive the *improvement rate* achieved when fetching instructions and operands with the 32-bit microprocessor? (10%)

9. The time delays associated with the *four* stages of an *instruction pipeline* are listed as follows: $\tau_1 = 45$ ns, $\tau_2 = 30$ ns, $\tau_3 = 85$ ns, and $\tau_4 = 40$ ns.
The time delay of a latch (or register) that forwards data to the next stage is $\tau_r = 3$ ns. (16%, 8% each)

(a) Compute the total execution time required for the 4-stage pipeline to perform 250 instructions. (8%)

(b) Show *a way* that can reduce the execution time to be about *one-half* of the time as required in part (a), for performing the same 250 instructions. You need justifying your answer. (8%)

10. Consider the following *two versions* of a program to add vectors, B and C, with *N* elements per vector. (24%, 8% each)

```
L1:       DO 15  i = 1, N
L2:           A(i) = B(i) + C(i)
L3:  15   CONTINUE
L4:       Sum = 0
L5:       DO 35  j = 1, N
L6:           Sum = Sum + A(j)
L7:  35   CONTINUE
```

```
        DOALL k = 1, M
          DO 15  i = (k – 1)L + 1, kL
              A(i) = B(i) + C(i)
15        CONTINUE
          Sum(k) = 0
          DO 35  j = 1, L
              Sum(k) = Sum(k) + A(j + (k – 1)L)
35        CONTINUE
        ENDALL
```

(a) The *left-version* program executes on a ***uniprocessor***. Suppose each line of code L2, L4, and L6 takes ***one*** processor clock cycle to execute. We *ignore* the time required for the other lines of code. Initially all arrays are loaded in main memory and the short program fragment is ready in the instruction cache. How many clock cycles are required to execute this program on a uniprocessor? (8%)

(b) The *right-version* program is executed on a ***multiprocessor*** with *M* processors. We partition the looping operations into *M* sections with $L = N/M$ elements per section. **DOALL** declares that all *M* sections are executed in parallel. The result of this program is to produce *M* partial sums. Assume that ***p*** clock cycles are needed for each interprocessor communication operation via the shared memory and that thus the addition of each partial sum requires ***p*** cycles. An ***m***-level binary adder tree is applied to merge all the partial sums, where $m = \log_2 M$. What are the total cycles needed to perform the final sum? (8%)

(c) Assume that $N = 2^{18}$ elements in the array, $M = 128$ processors, and $p = 120$. What is the *speedup* achieved by using the multiprocessor? (8%)