

115EE06

國立臺北科技大學 115 學年度碩士班招生考試

系所組別：2151 電機工程系碩士班戊組

第一節 數位邏輯設計 試題 (選考)

第 1 頁 共 1 頁

注意事項：

1. 本試題共 8 題，共 100 分。
2. 不必抄題，作答時請將試題題號及答案依照順序寫在答案卷上。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

I. (10%) Consider two numbers as follows:

$$A = 52_8$$

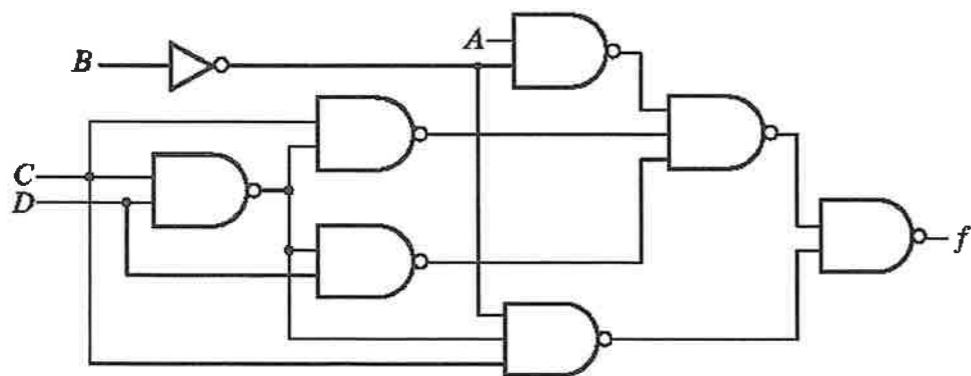
$$B = 20_{11}$$

- (i) Convert the following two numbers to binary. (3%)
- (ii) convert two binary numbers to $(-A)$ and $(-B)$ by assuming that negative numbers are represented in 2's complement with 7 bits and the most significant bit represents the positive or negative sign. (2%)
- (iii) Perform $(-A) + (-B)$ in binary and indicate when an overflow occurs. (5%)

II. (15%) Reduce the following expression to a *minimal* sum-of-product terms.

- (i) $abd'f + b'cegh' + abd'f + acd'e + b'ce$ (5%)
- (ii) $(a' + c + d)(a' + b + e)(a + c' + e')(c + d + e')(b + c + d' + e)(a' + b' + c + e')$ (5%)
- (iii) $f(a, b, c, d) = \sum m(1, 3, 4, 11) + \sum d(2, 7, 8, 12, 14, 15)$ (5%)

III. (10%) Convert the above circuit into a four-level circuit only containing AND and OR gates and a minimum number of inverters.



IV. (10%) Redesign a Full Adder with the following components:



- (i) A Programmable Logic Array (PLA) table. (5%)
- (ii) A Read-Only Memory (ROM) (5%)

V. (10%) An AB latch operates as follows: If $A = 0$ and $B = 0$, the next latch state is $Q^+ = 1$; if $A = 0$ and $B = 1$, the next latch state is $Q^+ = 0$; if $A = 1$ and $B = 0$, the latch output does not change; and the input combination $A = 1$ and $B = 1$ is not allowed.

- (i) Draw a circuit for the AB latch with two-input NOR gates. (5%)
- (ii) Use a SR latch to design the AB latch. (5%)

VI. (20%) Consider a counter which counts in the following sequence:

$$CBA = 000, 001, 011, 111, 101, 100, (\text{repeat}) 000, \dots$$

- (i) Design the above counter with D, T, JK flip-flops to store C, B, and A (15%)
- (ii) What will happen if the above counter was started in 010? (5%)

VII. (10%) A sequential circuit has an input (X) and an output (Z). The output is the same as the input was two clock periods previously. For example,

$$X = 0101101011010001$$

$$Z = 0001011010110100$$

The first two values of Z are 0. Construct a Mealy state graph for the circuit.

VIII. (15%) Consider the following state machine with one input, X , one output, Z , and the states from A to I .

- (i) Is this a Moore or Mealy state machine (5%)
- (ii) Reduce the following state table to a minimum number of states (10%)

State	Input		Output
	$X = 0$	$X = 1$	
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	C	E	0