1155C04

國立臺北科技大學 115 學年度碩士班招生考試

系所組別：2240 電子工程系碩士班丁組

第一節　電子學　試題

注意事項：

1. 本試題共三大題，共 100 分。
2. 不必抄題，作答時請將試題題號及答案依照順序寫在答案卷上。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、(50%)選擇題（單選題，每題 5 分，共 10 題，合計 50 分）

1. About the α and β of a BJT, which of the following statements is true? (A) α is more sensitive to semiconductor process variations than β. (B) β is more sensitive to semiconductor process variations than α. (C) Both α and β are equally sensitive to semiconductor process variations. (D) Whether α or β is more sensitive to semiconductor process variations is not deterministic.
2. Which of the following changes on a PN junction can significantly increase the zero-bias junction capacitance? (A) Decreasing the doping on the more heavily doped side (B) Increasing the doping on the more heavily doped side (C) Decreasing the doping on the less heavily doped side (D) Increasing the doping on the less heavily doped side
3. If a metal wire has a sheet resistance of 5 ohms/square, what is the equivalent resistance of this wire when the length is 100 μm and the width is 5 μm? (A) 100 ohm (B) 130 ohm (C) 160 ohm (D) 190 ohm
4. Normally, which of the following statements is NOT the reason for having a source degeneration configuration? (A) to increase input resistance (B) to make voltage gain less dependent on g_m (C) to increase voltage gain (D) to enhance linearity
5. Which of the following concepts is similar to source degeneration? (A) collector degeneration (B) base degeneration (C) emitter degeneration (D) gate degeneration
6. What is the minimum number of transistors in a traditional CMOS 2-input NAND gate? (A) four (B) six (C) eight (D) ten
7. If a sinusoidal voltage source has an output impedance of 3+j4 ohm and a peak-to-peak amplitude of 1 V, what is the maximum power that can be delivered to a load? (A) 8.9 dBm (B) 10.2 dBm (C) 11.4 dBm (D) 16.2 dBm
8. What is the unit obtained by multiplying "farad" and "ohm"? (A) watt (B) henry (C) volt (D) second
9. An Op-Amp working in a negative feedback loop is found to suffer from insufficient phase margin. Which of the following solutions is most likely to improve the phase margin? (A) Doubling the frequency at which the magnitude of the loop gain equals unity (B) Pushing the lowest-frequency pole of the loop gain to a higher frequency (C) Lowering the magnitude of the loop gain at low frequencies (D) Adding more right-half-plane zeros to the loop
10. If we want to reduce an Op-Amp's output resistance, which of the following remedies is NOT useful? (A) Adding a source-follower configuration (B) Adopting an emitter-follower configuration (C) Using a common-drain configuration (D) Appending a common-source configuration

二、(30%) Fig. 1 shows the schematic of an amplifier. Assume that the rE (i.e., rπ/(1+β)) of the BJT in Fig. 1 is 36 ohm. Assume that the midband gain of the amplifier is $|A_m| \equiv |v_2/v_1|$ when C_1 and C_2 work as a short, and when C_t functions as an open. Please answer the following questions by performing appropriate analyses and calculations.

1、 Derive the frequency of the pole contributed by C_t. Please give your answer in the unit of "Hz." (6%)

2、 Derive the frequency of the zero contributed by C_t. Please give your answer in the unit of "Hz." (6%)

3、 Derive the resistance observed by C_t when v_1 is turned off. (6%)

4、 If we want to make the upper 3-dB cutoff frequency of the midband gain as high as possible, how should we design R_g when R_g is defined as $R_s//R_1//R_2$? Points will be awarded only if your answer includes complete and rigorous derivations. (6%)

5、 Following the previous sub-question, what is approximately the value of R_g that can push the upper 3-dB cutoff frequency of the midband gain to half the highest frequency that can be achieved by tuning R_g? Points will be awarded only if your answer includes complete and rigorous derivations. (6%)

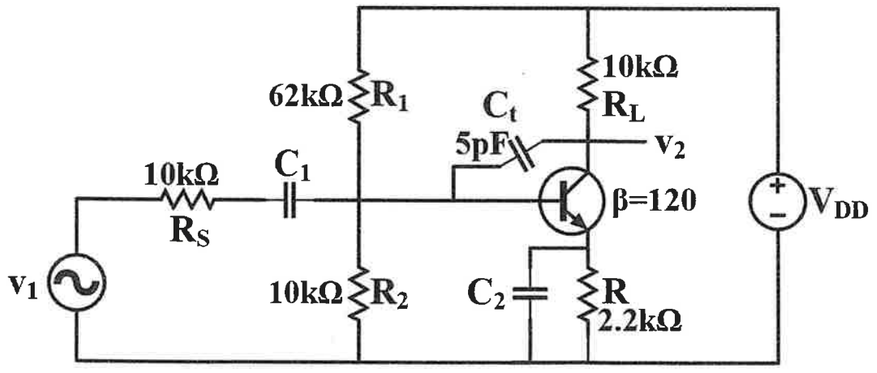

Fig. 1

注意：背面尚有試題

三、(20%) Fig. 2 shows the Bode magnitude plot of the loop gain of an amplifier with a pole at 2kHz. The low-frequency loop gain, $|T_{low}|$, is 20 dB as indicated by Fig. 2. When the open-loop amplifier is delivering full output power at 1kHz, the output stage develops 3% 2nd harmonic and 5% 3rd harmonic distortion. Please answer the following questions by performing appropriate analyses and calculations.

1、 Derive the magnitude of the loop gain at 2kHz. Please give your answer in "dB." (6%)

2、 Derive the magnitude of the loop gain at 3kHz. Please give your answer in "dB." (6%)

3、 Estimate the closed-loop total harmonic distortion (THD) of the amplifier at 1kHz. (8%)

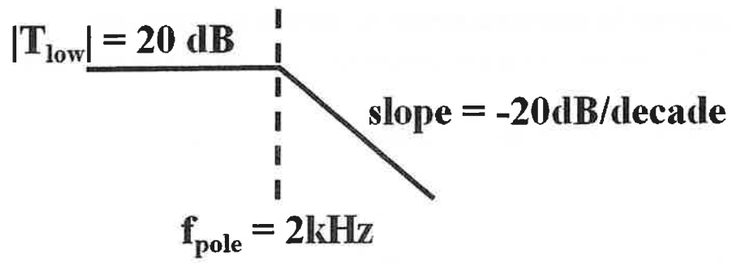

Fig. 2