國立臺北科技大學 100 學年度碩士班招生考試

系所組別：2401 光電工程系碩士班

第三節　電子學　試題（選考）

注意事項：

1. 本試題共五題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

[1] 20%

A short-base diode is one where the widths of the p and n regions are much smaller than L_n and L_p, respectively. As a result, the excess minority-carrier distribution in each region is a straight line rather than the exponentials shown in Fig. 1.

(a) For the short-base diode, sketch a figure corresponding to Fig. 1, and assume, as in Fig. 1, that $N_A >> N_D$. **(5%)**

(b) Show that if the widths of the p and n regions are denoted W_p and W_n then

$$I = Aqn_i^2\left[\frac{D_p}{(W_n - x_n)N_D} + \frac{D_n}{(W_p - x_p)N_A}\right]\left(e^{V/V_T} - 1\right)$$

and

$$Q_p = \frac{1}{2}\frac{(W_n - x_n)^2}{D_p} I_p \cong \frac{1}{2}\frac{W_n^2}{D_p} I_p, \text{ for } W_n >> x_n. \textbf{ (5%)}$$

(c) Also, assuming $Q \cong Q_p$, $I \cong I_p$, show that

$$C_d = \frac{\tau_T}{V_T} I$$

where

$$\tau_T = \frac{1}{2}\frac{W_n^2}{D_p}. \textbf{ (5%)}$$

(d) If a designer wishes to limit C_d to 8 pF at $I = 1$ mA, what should W_n be? Assume $D_p = 10$ cm^2/s. **(5%)**

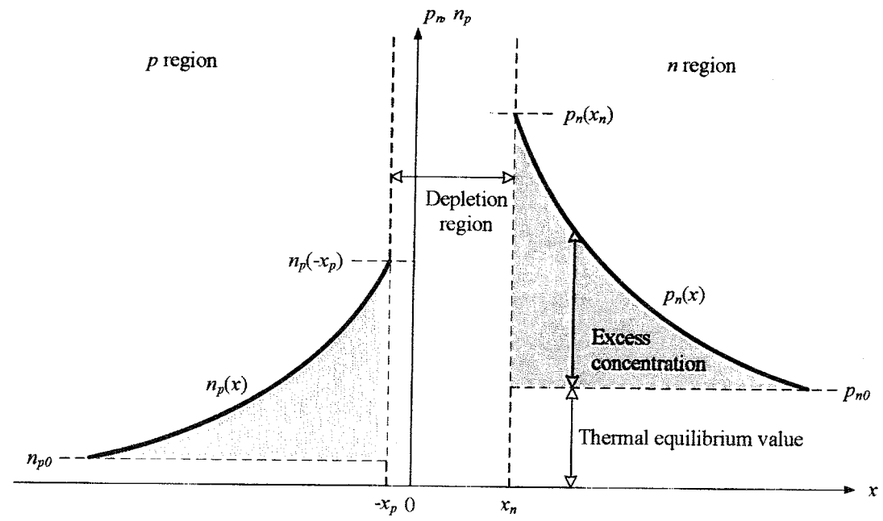

Fig. 1

[2] 20%

For the circuit of Figure 2, the OP-Amp has open-loop gain $A_d = 10^4$ V/V, differential input resistance $R_{id} = 100\text{K}\Omega$, and incremental output resistance $r_o = 1$ KΩ. Please use the feedback method to find:

(1)The voltage gain v_o/v_s. **(5%)**

(2)The input resistance R_{in}. **(5%)**

(3)The output resistance R_{out}. **(5%)**

(4)What is the configuration of the feedback amplifier? **(5%)**

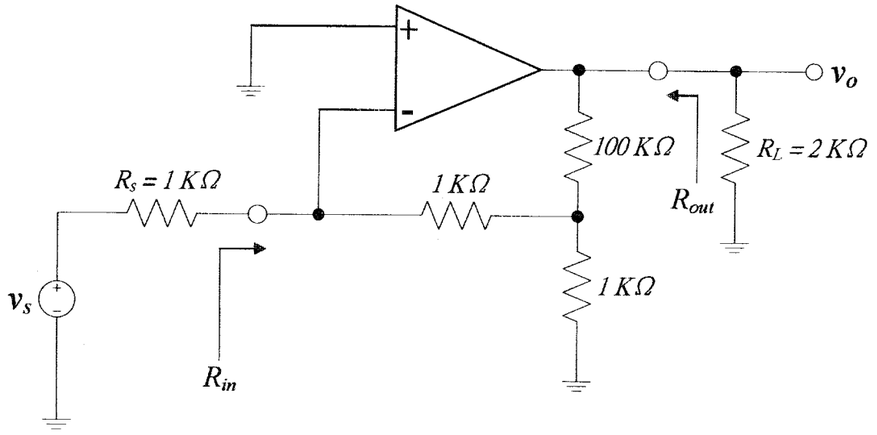

Fig. 2

注意：背面尚有試題

[3]　20%

For the circuit in Fig. 3, $|V_T|=1V$, $k'W/L=1mA/V^2$, $h_{fe}=100$, and the Early voltage magnitude for all devices (including those that implement the current sources) is $100V$. The signal source V_s has a zero dc component. Find the dc voltage at the output and at the base of Q_3. Find the values of A, β, A_f, R_{in} and R_{out}.

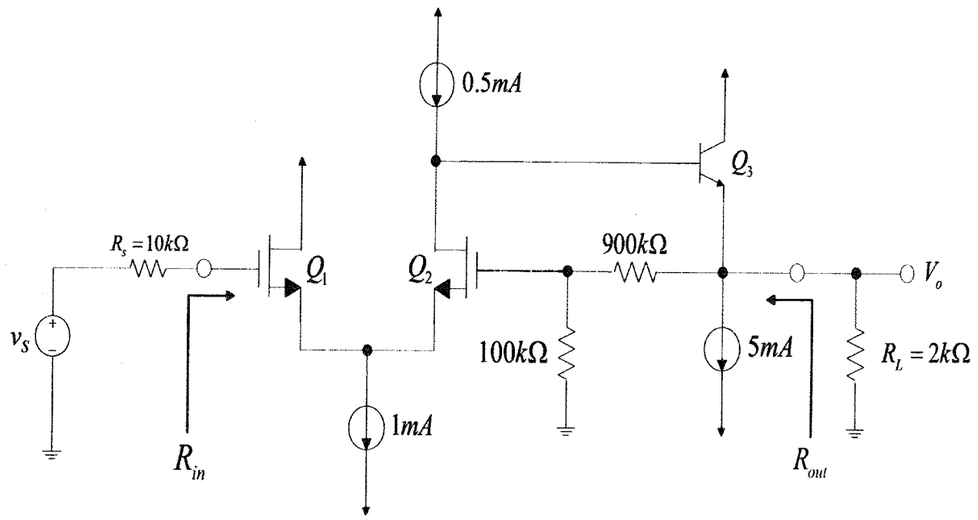

Fig. 3

[4]　20%

For the circuit of Fig. 4. Please find:

(1)The total gain $A_{db,total}$ of this complete filter. **(5%)**

(2)The bandwidth BW of this complete filter. **(5%)**

(3)The center frequency f_0 of this filter. **(5%)**

(4)Draw the Bode plot for the complete filter. **(5%)**

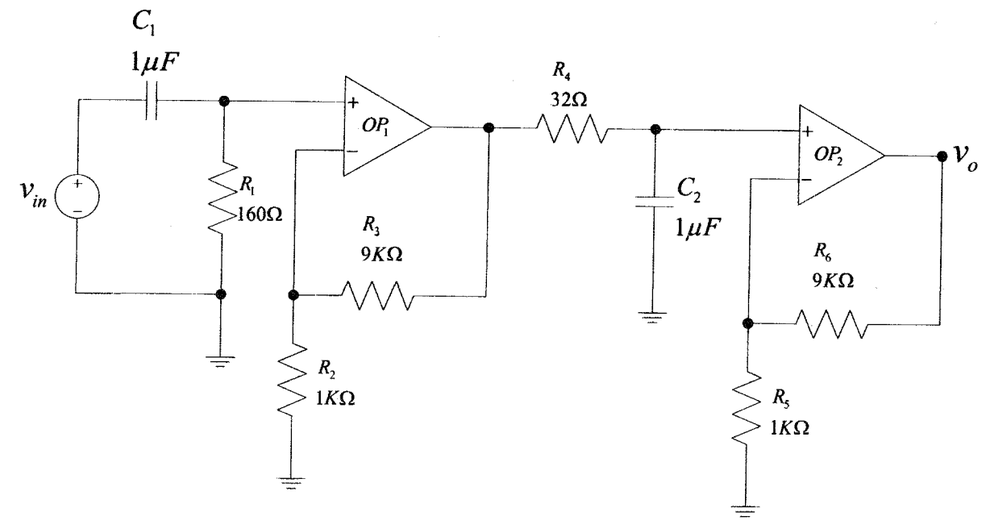

Fig. 4

[5]　20%

As shown in Figure 4, the schematic of a state-variable filter as shown contains passive elements and ideal operational amplifiers. Please derive the transfer functions of $V_1(S)/V_i(S)$ **(10%)**, and $V_3(S)/V_i(S)$. **(10%)**

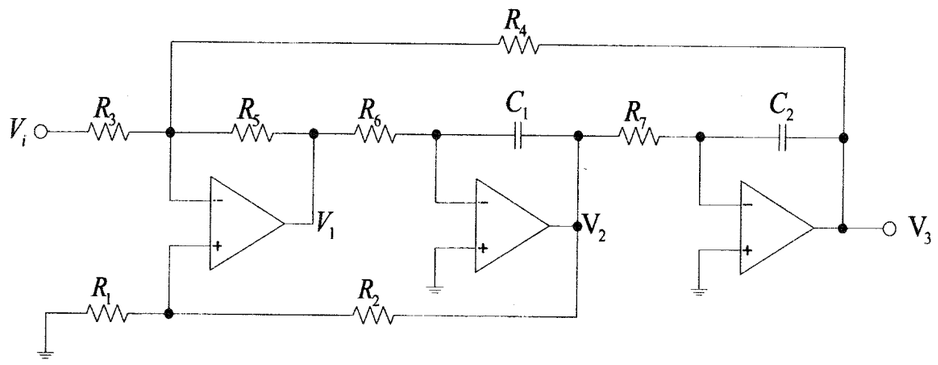

Fig. 5