國立臺北科技大學 111 學年度碩士班招生考試

系所組別：2152 電機工程系碩士班戊組

第一節　數位邏輯　試題（選考）

注意事項：

1. 本試題共八題，共 100 分。
2. 不必抄題，作答時請將試題題號及答案依照順序寫在答案卷上。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

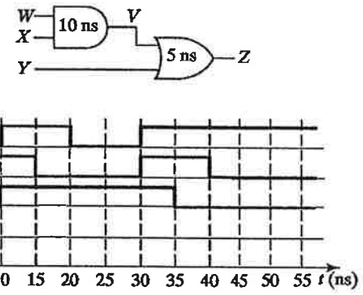
1. (10%) (a) $A = 101010$ and $B = 011101$ are 1's complement numbers. Perform $A - B$ and indicate whether overflow occurs. (5%)
   (b) Repeat part (a) assuming the numbers are 2's complement numbers. (5%)

2. (15%) Simplify the following expressions to a minimum sum of products. Only individual variables should be complemented.
   (a) $[(A' + B')' + (A'B'C)' + C'D\,]'$ (5%)
   (b) $(a' + c + d)(a' + b + e)\,(a + c' + e')\,(c + d + e')(b + c + d' + e)\,(a' + b' + c + e')$ (10%)

3. (10%) Find a minimum two-level, multiple-output AND-OR gate circuit to realize these functions.

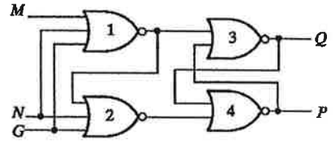
$$f_1(a, b, c, d) = \Sigma\, m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$$
$$f_2(a, b, c, d) = \Sigma\, m(2, 3, 5, 6, 7, 10, 11, 14, 15)$$
$$f_3(a, b, c, d) = \Sigma\, m(6, 7, 8, 9, 13, 14, 15)$$

4. (5%) Draw the timing diagram for V and Z for the circuit. Assume that the AND gate has delay of 10 ns and the OR gate has a delay of 5 ns.



5. (10%) Realize a full adder using a 3-to-8 line decoder with inverting outputs and two NAND gates.

6. (15%) The following circuit is intended to be a gated latch circuit where the signal G is the gate.
   (a) Derive the next-state equation for this circuit using Q as the state variable and P as an output. (10%)
   (b) Are there any restrictions on the allowable input combinations on M and N? Explain your answer. (5%)



7. (20%) Design a 3-bit counter which counts in the sequence:
   001, 011, 010, 110, 111, 101, 100, (repeat) 001, . . .
   (a) Use D flip-flops. (10%)
   (b) Use T flip-flops. (10%)

8. (15%) (a) Is the following circuit a Mealy or Moore state machine? (5%)
   (b) Construct a transition table or state graph for the following circuit. (10%)