

169 EE 07

國立臺北科技大學 109 學年度碩士班招生考試

系所組別：2152 電機工程系碩士班戊組

第一節 數位邏輯 試題 (選考)

第 1 頁 共 2 頁

注意事項：

1. 本試題共 11 題，共 100 分。
2. 不必抄題，作答時請將試題題號及答案依照順序寫在答案卷上。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

1. Perform the following conversion. You have to clearly show all your workings in your answer sheet.

- (a) [3 pts] Convert $(1234)_5$ to binary.
- (b) [3 pts] Convert $(F3C5)_{16}$ to octal.
- (c) [3 pts] Convert $(119.8125)_{10}$ to binary.
- (d) [3 pts] Convert $(1010101.101)_2$ to decimal.

2. Assuming the numbers are stored in 5-bit signed-2's complement representation. Perform each of the following operations and indicate whether an overflow error has occurred.

- (a) [4 pts] $00011 - 10011$
- (b) [4 pts] $11011 - 01011$
- (c) [4 pts] $11011 + 01011$

3. Consider the Boolean function

$$F(A, B, C, D) = \overline{A}CD + B\overline{C}D + ABC\overline{D} + \overline{A}BC\overline{D}$$

- (a) [5 pts] List the prime implicants for this function.
- (b) [2 pts] List the essential prime implicants for this function.
- (c) [3 pts] Find the minimal sum-of-products form for this function.

4. Consider the Boolean functions

$$F(A, B, C, D) = \sum m(0, 1, 2, 7, 8, 9) \text{ and } d = \sum m(3, 4, 5, 10, 13, 14),$$

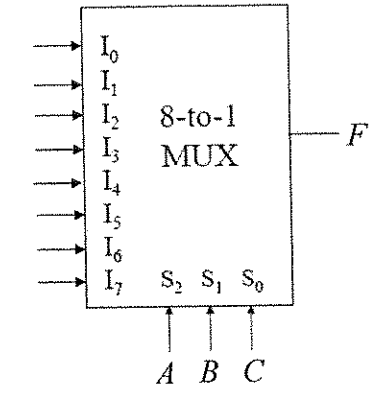
where d represents the don't care states that are part of F .

- (a) [3 pts] Use K-map to find the minimal sum-of-products form of F .
- (b) [3 pts] Use K-map to find the minimal product-of-sums form of F .

5. [8 pts] Implement the following Boolean function using an 8-to-1 multiplexer and a single inverter with variable D as its input.

$$F(A, B, C, D) = \sum m(1, 3, 4, 5, 10, 11, 12, 14)$$

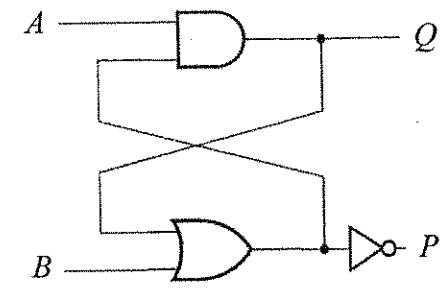
Copy and give the values of data inputs I_0, I_1, \dots, I_7 in the following diagram.



6. Design a magnitude comparator circuit for two 2-bit numbers A and B such that A and B are represented by A_1A_0 and B_1B_0 , respectively. If $A > B$, then the output function F is 1. If $A = B$, then the output function F is 0.

- (a) [5 pts] Construct the truth table.
- (b) [2 pts] Use K-map to find the minimal sum-of-products form of F .

7. Analyze the following new latch constructed from an AND gate, an OR gate, and an inverter.



Truth table

A	B	Q	Q ⁺
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

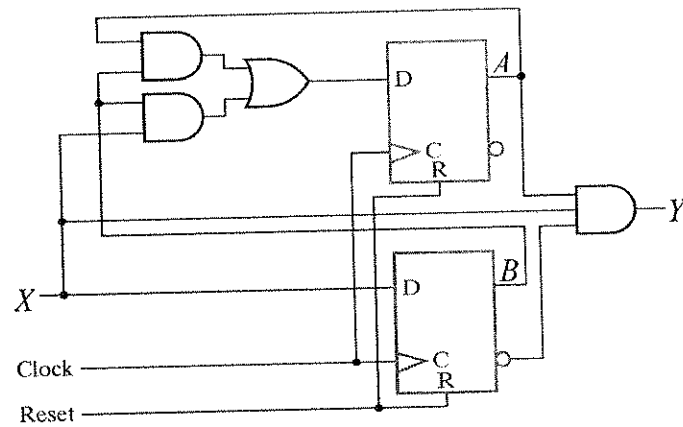
- (a) [8 pts] Copy and complete the above truth table for the new latch (where Q^+ represents the next state of Q).
- (b) [2 pts] What restriction must be placed on A and B so that P will always equal complement of Q ?

8. Design a 3-bit binary counter that goes through the sequence $010 \rightarrow 110 \rightarrow 001 \rightarrow 111$ and then repeat. Implement the counter using three D flip-flops $A, B,$ and C .

- (a) [5 pts] Find the state table for the circuit.
- (b) [3 pts] Find the flip-flop input equations $D_A, D_B,$ and D_C in minimal sum-of-products forms.
- (c) [2 pts] Indicate what happens if the circuit initially is in the unused state 000.

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9. Consider the following sequential circuit with two D flip-flops A and B , one input X , and one output Y .



State table for the circuit

Present State		Input X	Next State		Output Y
A	B		A^+	B^+	
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

- (a) [5 pts] Copy and complete the above the state table.
- (b) [2 pts] Is this a Mealy or a Moore circuit? Explain your answer.
- (c) [3 pts] List the output values of Y produced by the input sequence $X=1110110110$ (most significant bit input first).
10. [5 pts] A serial 2's completer circuit accepts a string of bits from the input X (least significant bit input first) and generates the corresponding 2's complement at the output Y . Please draw the state diagram using Mealy model for the circuit.
11. Consider a $128K \times 32$ SRAM memory chip organized in a rectangular array using a coincident selection scheme (using a row decoder and a column decoder) instead of a single row decoder.
- (a) [3 pts] What is the size of the row decoder?
- (b) [3 pts] What is the size of the column decoder?
- (c) [4 pts] Assume that the high order address bits go to the row decoder and that the low order address bits go to the column decoder. Determine the values of row selection lines when the input address is in hexadecimal $(1B7BF)_{16}$. Show your answer in hexadecimal notation.