國立臺北科技大學 100 學年度碩士班招生考試

系所組別：2300 資訊工程系碩士班

第一節　作業系統與計算機組織　試題

注意事項：

1. 本試題共 13 題，配分共 100 分。
2. 請標明大題、子題編號作答，不必抄題。
3. 全部答案均須在答案卷之答案欄內作答，否則不予計分。

一、Consider the following set of processes, with the arrival time and the length of the CPU-burst time given in milliseconds. What is the average waiting time for the following CPU scheduling algorithms? Please show how you calculate the answer.

Process	Arrival Time	Burst Time
P1	0	7
P2	2	4
P3	4	1
P4	5	4

1. The preemptive SJF (SRTF) scheduling algorithm. (4%)
2. The non-preemptive SJF scheduling algorithm. (4%)

二、For a system with 32-bit virtual addresses and 4 KB page size. Assume 4 bytes are used for each page table entry. Answer the following two questions.

1. If one-level page table implementation is used, how many bytes will be occupied by the page table for a 32MB process? (4%)
2. Now, a two-level page table design is used instead, in which a virtual address is divided into three fields: a 10-bit outer page number, a 10-bit inner page number, and a 12-bit page offset. If the minimum allocation unit for each (inner or outer) page table is one page, how many bytes will be occupied by the page table for a 32MB process? (6%)

三、Assume a process is allocated with three frames. What is the number of page faults for the LRU page replace algorithm if the page reference sequence is: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 4, 1, 2? (4%)

四、Given a disk with 200 tracks, numbered from 0 to 199. Assume the disk head is initially located at track 120 and was moving in the direction of increasing track number. Let the requested tracks, in the order received by the disk scheduler, be 55, 58, 39, 18, 90, 160, 150, 38, and 186. How many head movements will be involved for the C-LOOK disk scheduling algorithm? (4%)

五、Will all the requirements of the solution to the critical-section problem be satisfied for the following program? Please provide a brief discussion. (4%)

```
/* lock is a shared data and initialized to 0 */
while (1) {
  key = 1;
  while (key) {
    swap(lock, key); /* swap() is the atomic swap instruction */
  }
  ... the critical section part...
  lock = 0;
  ... the remaining part ...
}
```

六、Deadlock can be prevented by requiring that each process requests resources in an increasing order of enumeration. Why? (4%)

七、Message passing is a common method for developing parallel programs on distributed systems. Illustrate a major drawback for this mechanism. (4%)

八、Answer the following questions about multithreading.

1. Show one conditions in which multithreaded programs can't provide better performance. (4%)
2. Explain why local variables in a multithreaded program typically don't need to be protected by synchronization operations. (4%)

九、One difficulty for developing user-space device drivers in the Linux-based operating systems is that the hardware controllers can't be accessed in user space directly. Propose a method to solve this problem. (4%)

注意：背面尚有試題

十、(18%) For a typical MIPS processor with a five-stage pipeline, including (1)IF-Instruction fetch; (2) ID-Instruction decode and register fetch; (3)EX-Execution or calculate effective address; (4)MEM-Access data memory; and (5)WB-Write back to registers. Then, the following code segment will be executed using this pipeline.

i1: sub $5, $1, $3
i2: add $5, $4, $5
i3: and $2, $5, $6
i4: lw $3, 10($2)
i5: bne $5, $7, L1
i6: add $8, $9, $10
i7: sub $8, $8, $11
L1: lw $12, 12($8)

where *in* indicates the *n*th instruction in this code segment.

1. Please find all data dependencies in the above code segment in terms of *in.* (3%)
2. Identify all types of hazards in the above code segment in terms of *in.* (3%)
3. Please give the methods or techniques to resolve the hazards in the above question 2. (3%)
4. If we stall the pipeline when a data hazard happens (no forwarding), how many cycles will it take to complete the above code segment? Please illustrate the resulting pipeline. (5%)
5. Suppose the above MIPS code segment can be now executed using the logic of the data hazard detection and forwarding unit depicted in Figure 1. Please determine whether the above MIPS instructions are correctly executed? If so, please give your explanations. If not so, how can we revise and correct the logic in Figure 1 and so that the codes can be correctly executed? (4%)

```
If   (MEM/WB.RegWrite
       and (MEM/WB.RegisterRd ≠ 0 )
       and (MEM/WB.RegisterRd = ID/EX.RegisterRs ) )
Then
       ForwardA = 01

If   (MEM/WB.RegWrite
      and (MEM/WB.RegisterRd ≠ 0 )
      and (MEM/WB.RegisterRd = ID/EX.RegisterRt ) )
Then
       ForwardB = 01
```

Figure 1. The logic of the data hazard detection and forwarding unit

十一、(12%) Suppose we have two caches below, and each of which comprises of 32 words. Below is a sequence of memory address references as word addresses:

Address Sequence	**0, 55, 66, 18, 3, 101, 183, 55, 66, 226, 2, 100**

Please indicate each reference as a hit or a miss for the following two caches (a) and (b). Assuming that LRU(Least Recently Used) is used for each replacement algorithm and all the caches are initially empty.

1. Cache (a): For a direct-mapped cache with 8 four-word blocks, please indicate each reference as a hit or a miss, and determine its miss rate. (4%)
2. Cache (b): For a four-way set associative cache with two-word blocks, please indicate each reference as a hit or a miss, and determine its miss rate. (4%)
3. For each of above (a) and (b) caches, how many misses are conflict misses? (2%)
4. For each of above (a) and (b) caches, how many misses are compulsory misses? (2%)

十二、(8%) Given the following hardware components in Figure 2, including one 8-bit register, one 8-bit ALU, one 16-bit shift register, and a control unit.

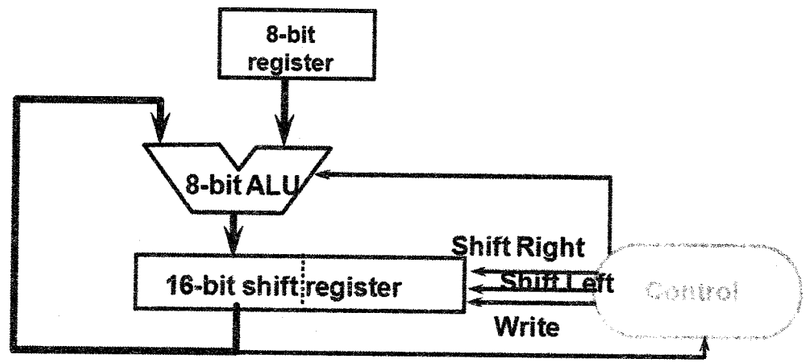

Figure 2. The logic of the data hazard detection and forwarding unit

1. Given the above hardware components in Figure 2, can you design a combinative hardware for both multiplication and division computations on 8-bit integers? Please sketch your design (hints: Multiplication needs Multiplicand, Multiplier, and Product; Division needs Dividend, Divisor, Quotient, and Remainder). (3%)
2. Given the two decimal numbers in the following table.

A	B
183_{10}	56_{10}

Can you calculate A divided by B (A÷B) using your designed combinative hardware? Please show the contents of each of the three registers (Divisor, Quotient, and Remainder) on each step. (5%)

十三、(12%) The following C code segments in Figure 3 compute matrix multiplications of two integer matrices A and B, where A is a 1×128 row matrix, and B is a 128×4 matrix.

C-1	for (i = 0; i < 128; i++)
	  for (j = 0; j < 4; j++)
	  C[j] += A[i] * B[j][i];

C-2	for (j = 0; j < 4; j++)
	  for (i = 0; i < 128; i++)
	  C[j] += A[i] * B[j][i];

Figure 3. The C code segments for matrix multiplication

1. What are the accuracies (in percentage) of "always-taken" and "always-not-taken" predictors for the outer and inner loops in the above two code segments, respectively? (4%)
2. What are the accuracies of the two-bit predictor in the following Figure 4 for the branches for the outer and inner loops in the above two code segments, respectively? Assume that the predictor starts off in the bottom-left state in Figure 4 (predict not taken). (4%)

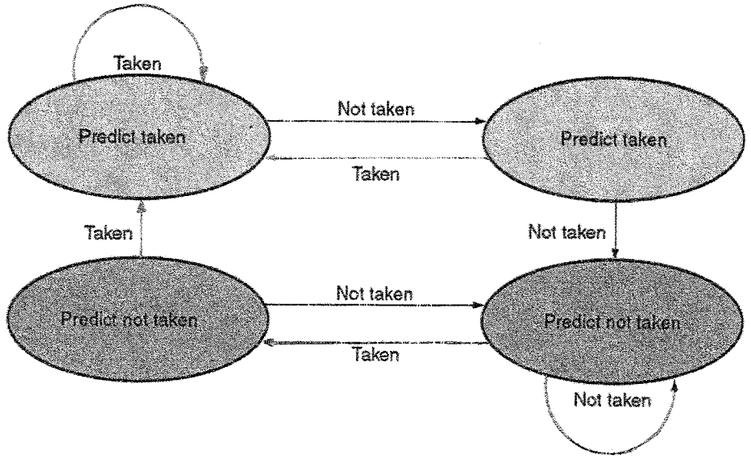

Figure 4. The two-bit predictor

3. The elements within the same row are contiguously stored in the C program. Therefore, given a cache with four-word blocks, references to which variables in the above code segments in Figure 3 can reveal spatial locality? (2%)
4. Similar to the above question 3, references to which variables in the above code segments in Figure 3 can reveal temporal locality? (2%)